



QUALCOMM® QUICK CHARGE™ 3.0 TECHNOLOGY

CERTIFICATION TEST REPORT

FOR

POWER BANK

MODEL NUMBER: UP-9065

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Prepared for

Prepared by

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Revision History

Rev.	Issue Date	Revisions	Revised By
--	2017/10/18	Initial Issue	D. Chiang

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1. ATTESTATION OF TEST RESULTS

COMPANY NAME:

EUT DESCRIPTION: POWER BANK

MODEL: UP-9065

SERIAL NUMBER: Prototype

DATE TESTED: October 10, 2017

APPLICABLE STANDARDS	
STANDARD	TEST RESULTS
High Voltage Dedicated Charging Port Interface Specification Revision K	Pass

UL Verification Services (Guangzhou) Co., Ltd., Song Shan Lake Branch tested the above equipment in accordance with the requirements set forth in the above standards. All indications of Pass/Fail in this report are opinions expressed by UL Verification Services (Guangzhou) Co., Ltd., Song Shan Lake Branch based on interpretations and/or observations of test results. Measurement Uncertainties were not taken into account and are published for informational purposes only. The test results show that the equipment tested is capable of demonstrating compliance with the requirements as documented in this report.

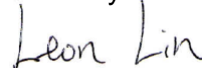
Note: The results documented in this report apply only to the tested sample, under the conditions and modes of operation as described herein. This document may not be altered or revised in any way unless done so by UL Verification Services (Guangzhou) Co., Ltd., Song Shan Lake Branch and all revisions are duly noted in the revisions section. Any alteration of this document not carried out by UL Verification Services (Guangzhou) Co., Ltd., Song Shan Lake Branch will constitute fraud and shall nullify the document. This report must not be used by the client to claim product certification, approval, or endorsement by Qualcomm.

Approved & Released For
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Tested By:



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ENGINEER
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2. TRADEMARK NOTICES

Qualcomm is a trademark of Qualcomm Incorporated, registered in the United States and other countries. Qualcomm Quick Charge is a trademark of Qualcomm Incorporated. All Qualcomm Incorporated marks are used with permission.

3. TEST METHODOLOGY

The tests documented in this report were performed in accordance with High Voltage Dedicated Charging Port HVDCP Compliance Plan Revision D as amended by instructions from Qualcomm.

4. FACILITIES AND ACCREDITATION

The test sites and measurement facilities used to collect data are located at Building 10, Innovation Technology Park, Song Shan Lake Hi-Tech Development Zone, Dongguan, 523808, China.

The Laboratory has been assessed and proved to be in compliance with CNAS, The Certificate Registration Number is L9923.

Notes:

1. All measurements documented in this report are outside the scope of the Laboratory's accreditation.
2. The Laboratory used for performing the measurements documented in this report is third party accredited to ISO 17025.

5. CALIBRATION AND UNCERTAINTY

5.1. MEASURING INSTRUMENT CALIBRATION

The measuring equipment utilized to perform the tests documented in this report has been calibrated in accordance with the manufacturer's recommendations, and is traceable to recognized national standards.

5.2. TEST AND MEASUREMENT EQUIPMENT

The following test and measurement equipment was utilized for the tests documented in this report:

TEST EQUIPMENT LIST					
Description	Manufacturer	Model	Asset	Cal Date	Cal Due
Multimeter	FLUKE	114	--	24/12/2016	24/12/2017
Oscilloscope	Teledyne Lecroy	HDO6034	LCRY3651N18536	24/12/2016	24/12/2017
Electronic Load	Chroma	63610-80-20	636002001123	24/12/2016	24/12/2017
SourceMeasure Unit	Keithley	2602B	4091402	1/4/2017	1/4/2018
Current Probe	Teledyne Lecroy	CP030	--	1/4/2017	1/4/2018

6. EQUIPMENT UNDER TEST

6.1. DESCRIPTION OF EUT

The EUT is a QUALCOMM® Quick Charge™ 3.0 charger.

It is a power bank

Input power is furnished by USB Power

Power can also be provided by a battery.

The rated output current at each output voltage is as follows:

Output Voltage (Volts)	Rated Current (Amps)
5	3.0
9	2.0
12	1.5

Rated Current at Load Point B (Amps)
2.5

HVDCP detection is performed by a micro controller.

The chipset performing the HVDCP detection is U1, mfr. INJOINIC, part number IP5318A.

The Quick Charge output is furnished via a USB Type A connector

Normal port:

Port No. (In turn)	Output Voltage (Volts)	Rated Current (Amps)
2	5	3

The QC port will be became normal condition when normal port is used. The test in 7.3.1 is considered QC port condition.

There is Input/ output function for USB Type C connector.

NOTE:

Revised the parameter of Tv_cont_change from 2ms to 30ms due to approval of Qualcomm email on 2017-09-29

7. TEST RESULTS

7.1. HVDCP Insertion

7.1.1. D+/D- Shorting Time

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Measured Value (ms)	Maximum Limit (ms)	Pass/Fail
Td+_d-_short	Vbus >= 0.8 V (Min Votg_sess_vld)	D- >= 0.5 V (Min Vdm_src)	13.102	20	PASS

WAVEFORM AND MEASUREMENTS



7.1.2. D+/D- Remains Shorted at 3.3 V

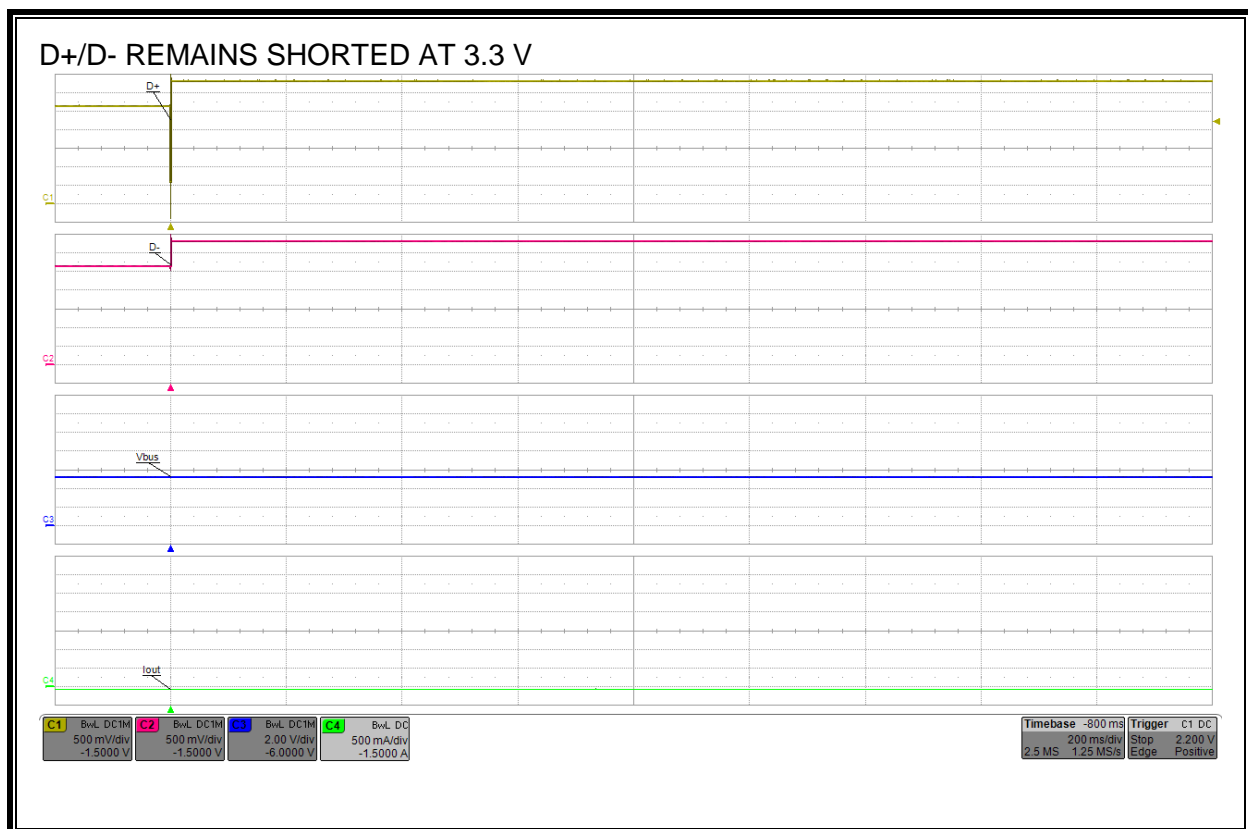
LIMITS AND RESULTS

Requirement: D- remains shorted to D+ when D+ is set to 3.3 V and D- Floats

Beginning 1.5 seconds (Max Tglitch_bc_done) after D+ \geq 2.2 V (Max Vsel_ref), confirm D- \geq 2.2 V (Max Vsel_ref)

Parameter	Measured Value (V)	Minimum Limit (V)	Pass/Fail
D-	3.30	2.2	PASS

WAVEFORM AND MEASUREMENTS



7.2. HVDCP Negotiation

7.2.1. One Second Glitch Filter

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Measured Value (s)	Minimum Limit (s)	Maximum Limit (s)	Pass/Fail
Tglitch_bc_done	D+ >= 0.4 V (Max Vdat_ref)	D- <= 0.25 V (Min Vdat_ref)	1.25	1.0	1.5	PASS

WAVEFORM AND MEASUREMENTS



7.2.2. Rdcg_dat

LIMITS AND RESULTS

Measured D+ Voltage (V)	Measured D- Voltage (V)	Measured D+ Current (mA)	Rdcg_dat Measured Value (ohms)	Rdcg_dat Maximum Limit (ohms)	Pass/Fail
0.600	0.566	0.949	35.5	40	PASS

7.2.3. Rdm_dwn

LIMITS AND RESULTS

Parameter	Measured Value (k ohms)	Minimum Limit (k ohms)	Maximum Limit (k ohms)	Pass/Fail
Rdm_dwn	17.550	14.25	24.80	PASS

7.2.4. Rdat_lkg

LIMITS AND RESULTS

Parameter	Measured Value (k ohms)	Minimum Limit (k ohms)	Maximum Limit (k ohms)	Pass/Fail
Rdat_lkg	317.5	300	1500	PASS

7.3. Portable Device Request Recognition

7.3.1. Output Voltage

LIMITS AND RESULTS

Output Voltage at No Load					
Nominal Vbus (V)	Load Current (A)	Measured Vbus (V)	Minimum Limit (V)	Maximum Limit (V)	Pass/Fail
5	0.0	5.21	4.75	5.50	PASS
9	0.0	9.25	8.55	9.90	PASS
12	0.0	12.17	11.40	13.20	PASS

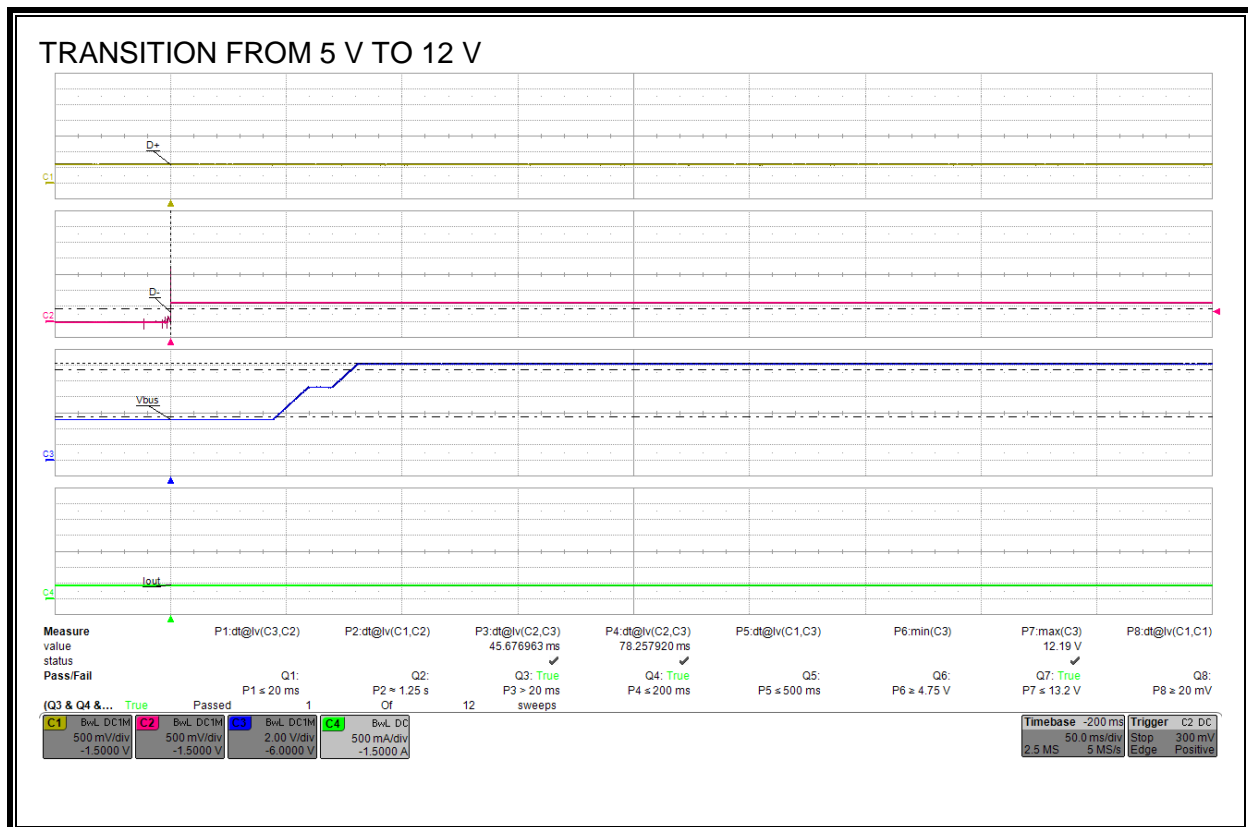
Output Voltage at Max Rated Load				
Nominal Vbus (V)	Load Current (A)	Measured Vbus (V)	Minimum Limit (V)	Pass/Fail
5	3.00	5.05	4.75	PASS
9	2.00	9.13	8.55	PASS
12	1.50	12.09	11.40	PASS

7.3.2. Transition from 5 V to 12 V

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Meas Value (ms)	Min Limit (ms)	Max Limit (ms)	Pass/Fail
Tglitch_mode_change	D- \geq 0.4 V (Max Vdat_ref)	Vbus \geq 5.5 V (Max Vbus_5v)	45.67	20	60	PASS
Tv_new_request	D- \geq 0.4 V (Max Vdat_ref)	Vbus \geq 11.4 V (Min Vbus_hv)	78.25		200	PASS

WAVEFORM AND MEASUREMENTS

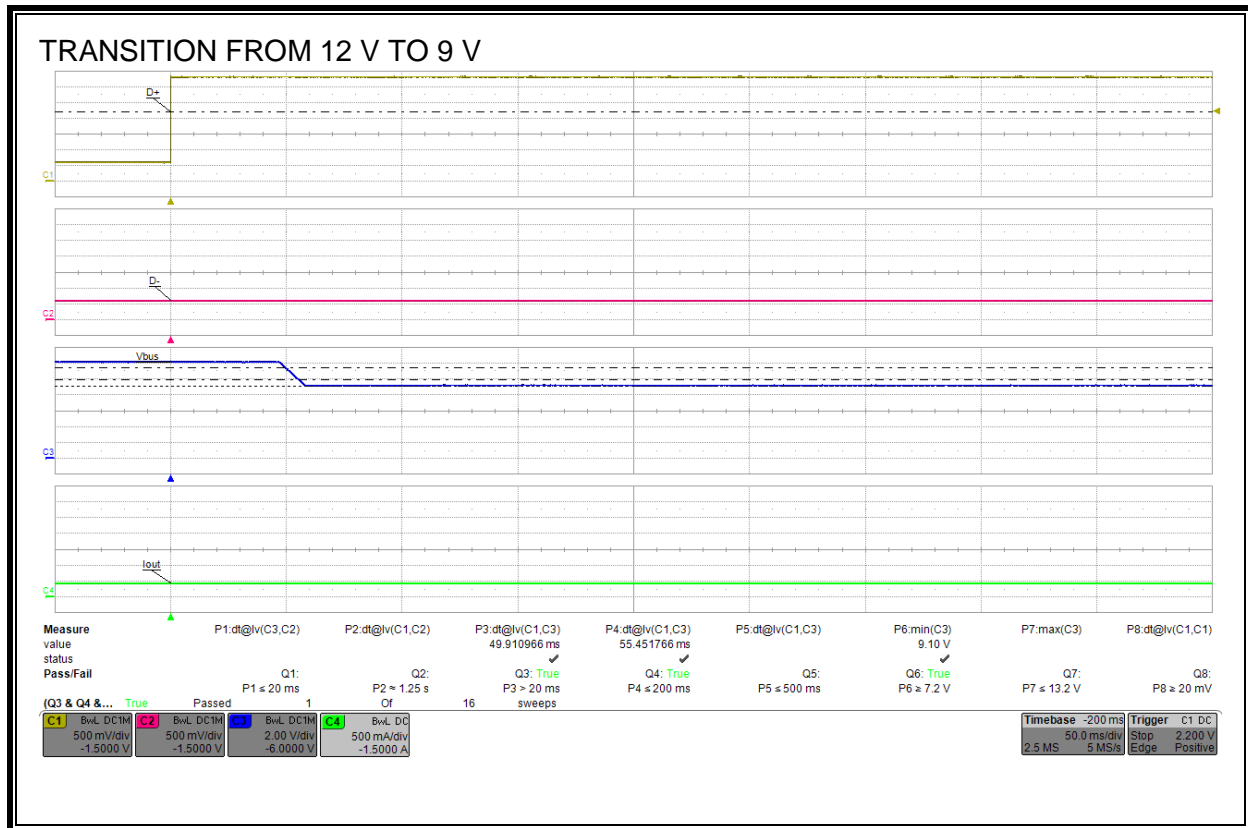


7.3.3. Transition from 12 V to 9 V

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Meas Value (ms)	Min Limit (ms)	Max Limit (ms)	Pass/Fail
Tglitch_mode_change	D+ >= 2.2 V (Max Vsel_ref)	Vbus <= 11.4 V (Min Vbus_hv)	49.91	20	60	PASS
Tv_new_request	D+ >= 2.2 V (Max Vsel_ref)	Vbus <= 9.9 V (Max Vbus_hv)	55.45		200	PASS

WAVEFORM AND MEASUREMENTS



7.3.4. Maintain 9 V with Reserved Request

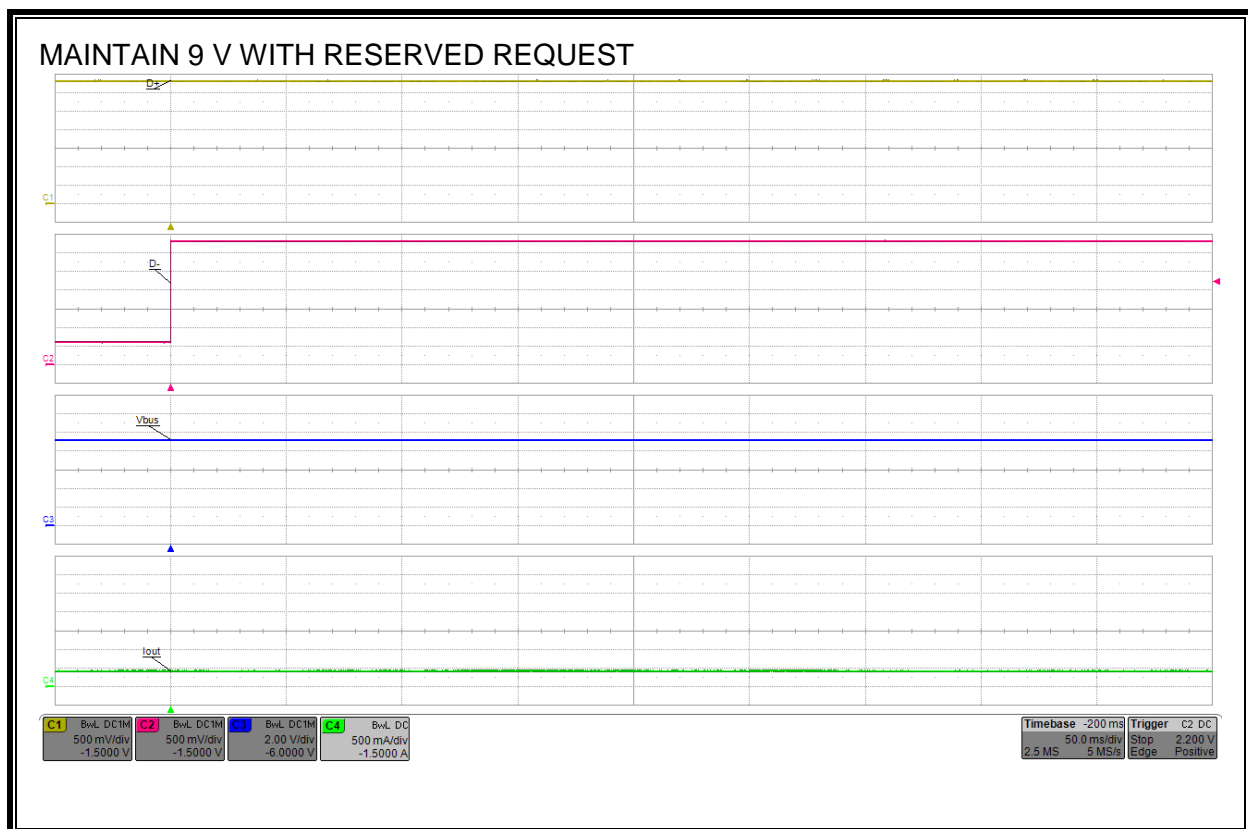
LIMITS AND RESULTS

Initial Condition: Vbus is 9 volts

Observation Period: Monitor for longer than 200 ms (Max Tv_new_request) after Reserved Request is asserted

Parameter	Measured Value (V)	Minimum Limit (V)	Maximum Limit (V)	Pass/Fail
Vbus	9.197	8.55	9.90	PASS

WAVEFORM AND MEASUREMENTS



7.3.5. Maintain 9 V with Continuous Request

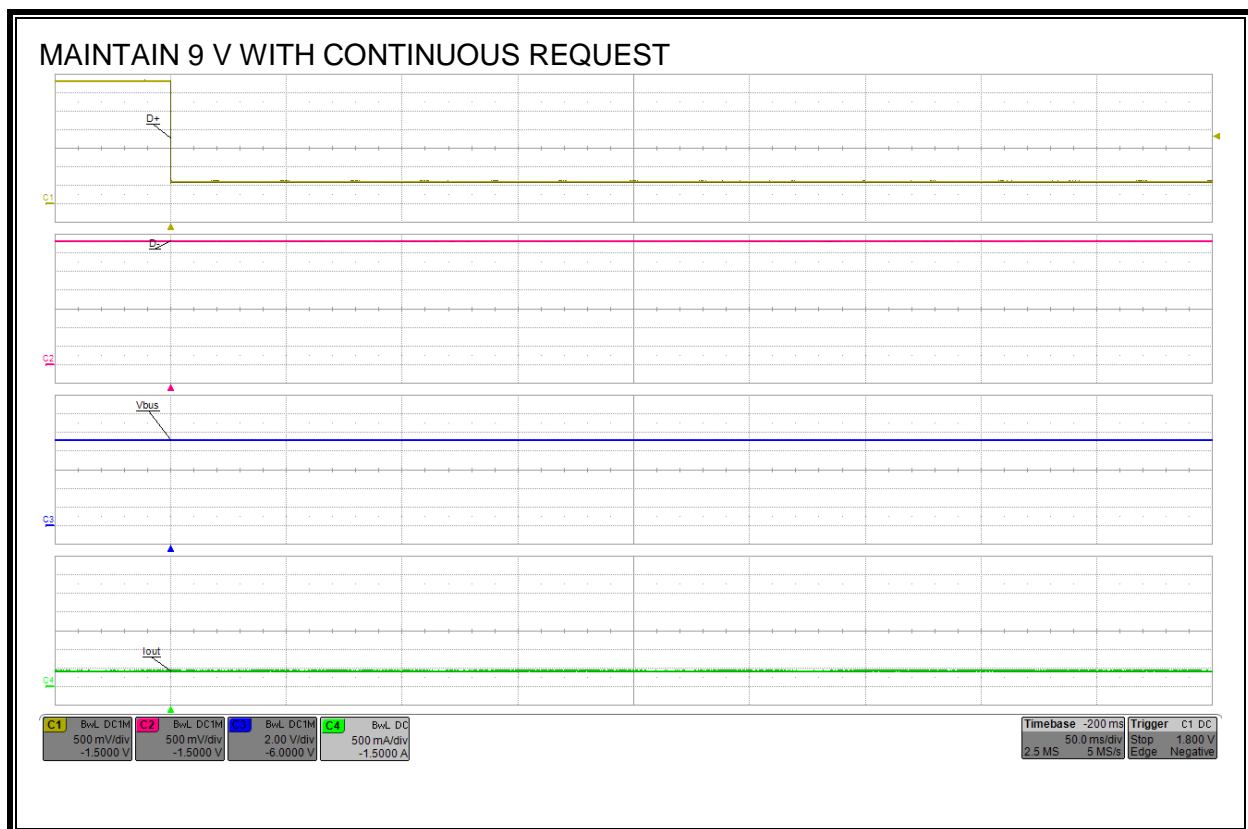
LIMITS AND RESULTS

Initial Condition: Vbus is 9 volts

Observation Period: Monitor for longer than 200 ms (Max Tv_new_request) after Continuous Request is asserted

Parameter	Measured Value (V)	Minimum Limit (V)	Maximum Limit (V)	Pass/Fail
Vbus	9.197	8.55	9.90	PASS

WAVEFORM AND MEASUREMENTS

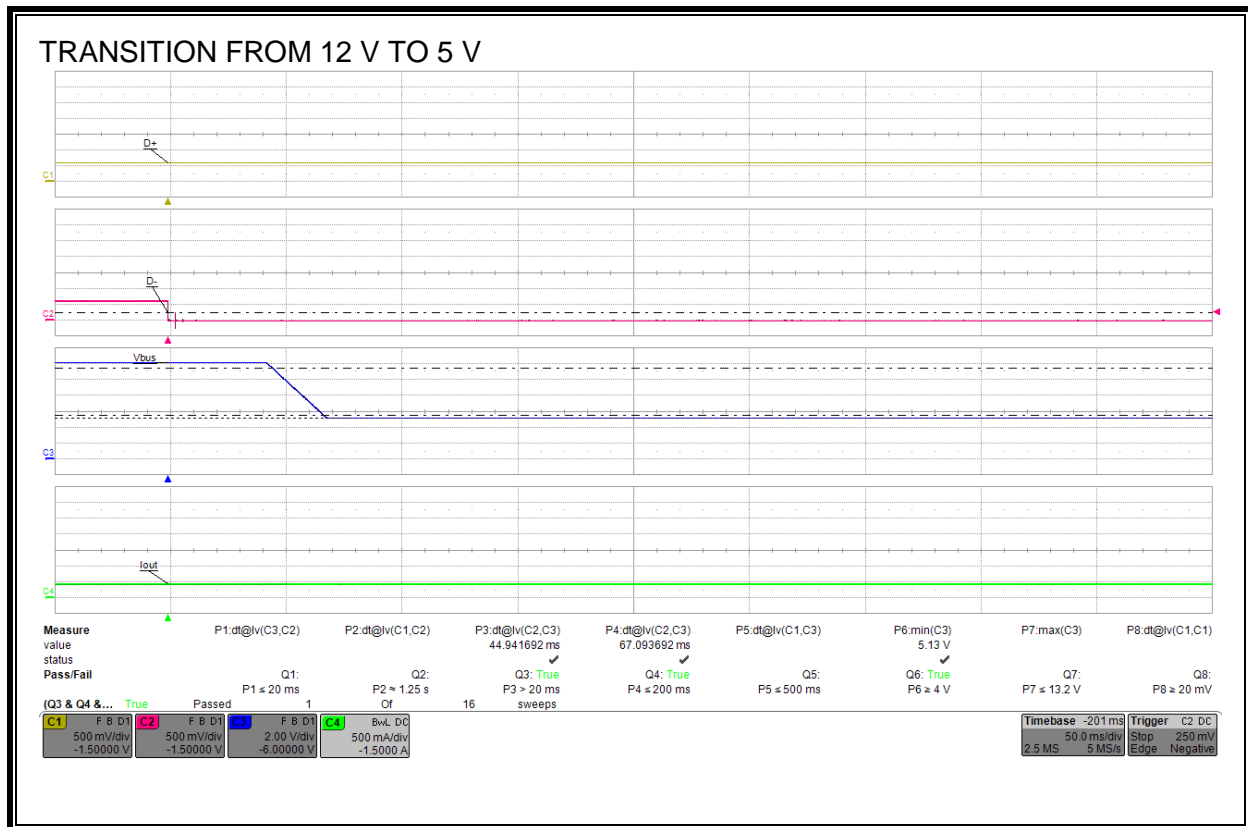


7.3.6. Transition from 12 V to 5 V

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Meas Value (ms)	Min Limit (ms)	Max Limit (ms)	Pass/Fail
Tglitch_mode_change	D- <= 0.25 V (Min Vdat_ref)	Vbus <= 11.4 V (Min Vbus_hv)	44.94	20	60	PASS
Tv_new_request	D- <= 0.25 V (Min Vdat_ref)	Vbus <= 5.5 V (Max Vbus_5v)	67.09		200	PASS

WAVEFORM AND MEASUREMENTS



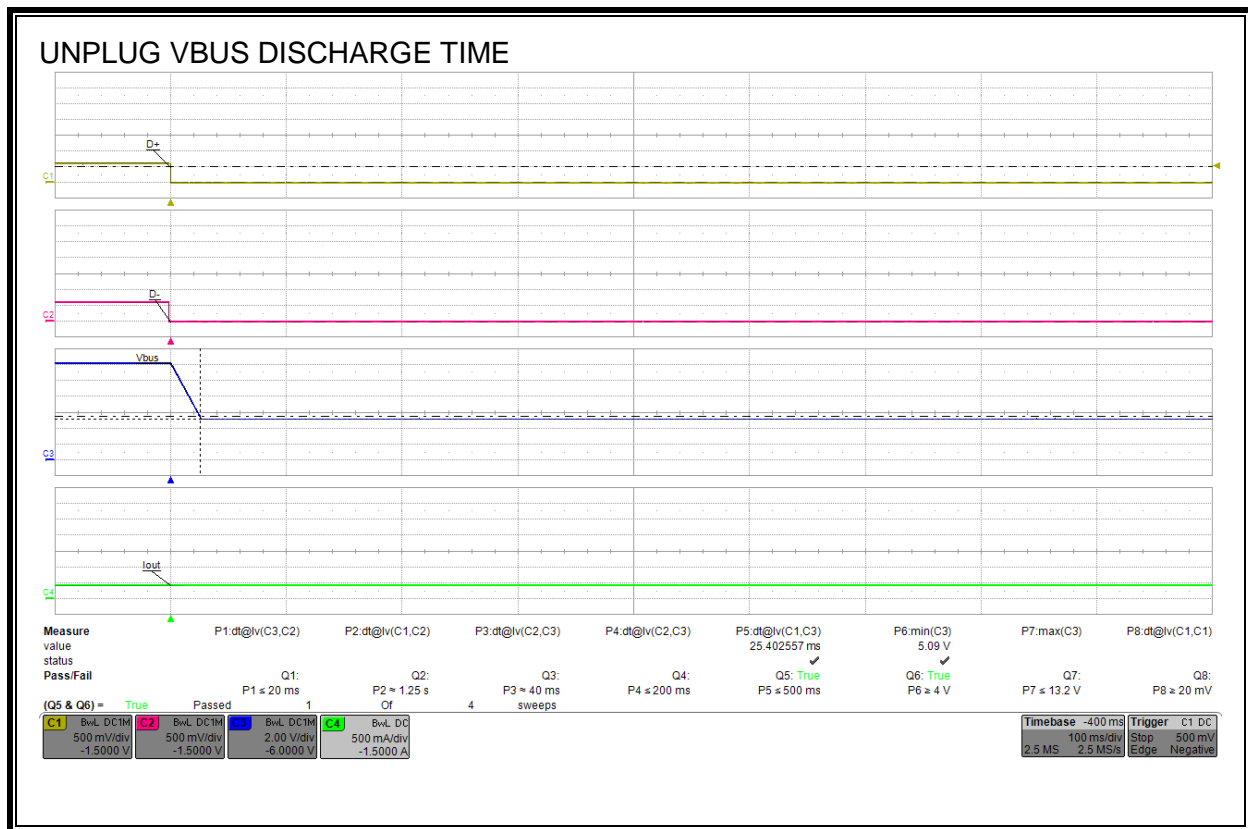
7.4. Portable Device Removal

7.4.1. Unplug Vbus Discharge Time

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Measured Value (ms)	Maximum Limit (ms)	Pass/Fail
Tv_unplug	D+ <= 0.5 V (Min Vdp_src)	Vbus <= 5.5 V (Max Vbus_5v)	25.40	500	PASS

WAVEFORM AND MEASUREMENTS



7.5. Portable Device USB PHY Error Rejection

7.5.1. Square Wave Error Rejection

LIMITS AND RESULTS

Initial Condition: Vbus is 5 volts

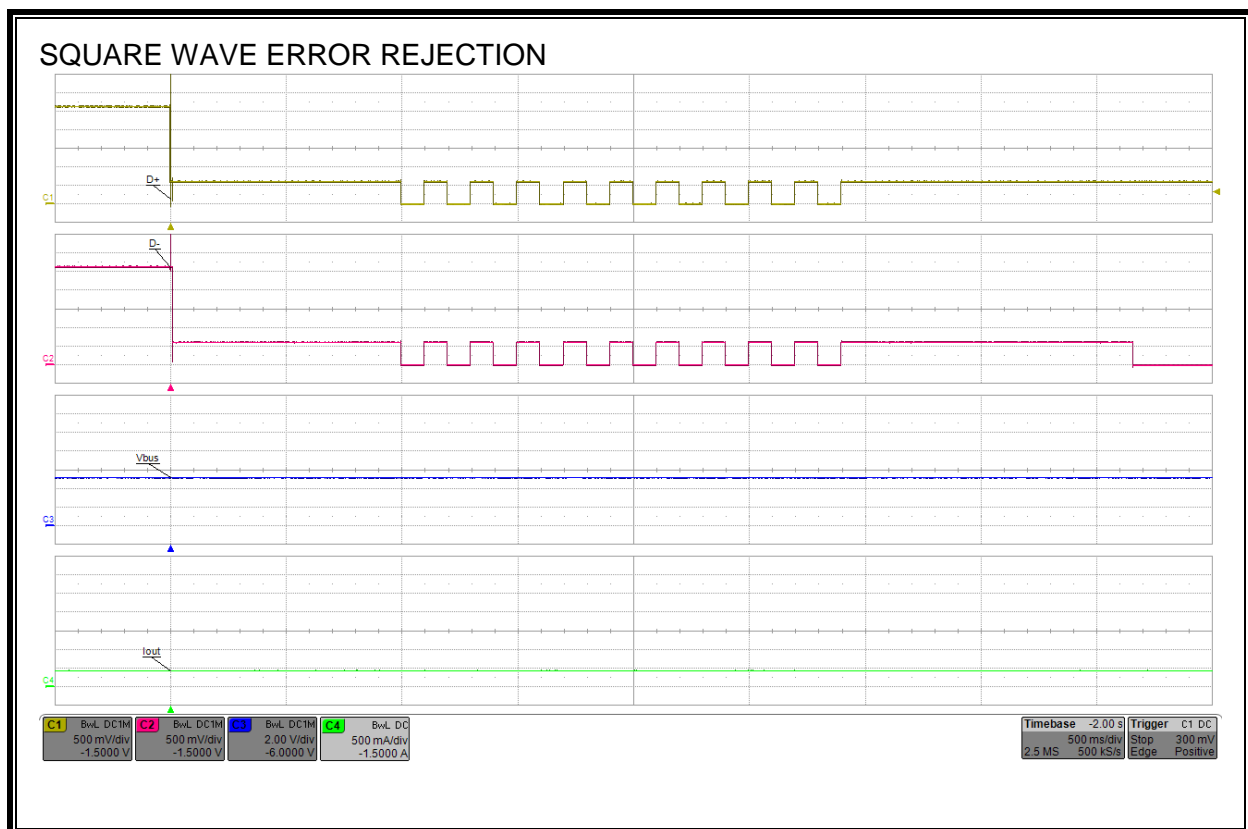
Applied Waveform: D+ = 0.6 V for 990 ms, then 0.6 V / 0 V pulse train, then remains at 0.6 V

Requirements: D- tracks D+ until Tglitch_bc_done after the completion of the pulse train, and Vbus remains at 5 volts

Observation Period: Monitor until at least 1.5 seconds after pulse train

Parameter	Measured Value (V)	Minimum Limit (V)	Maximum Limit (V)	Pass/Fail
D+/ D- Tracking				PASS
Vbus	5.165	4.75	5.50	PASS

WAVEFORM AND MEASUREMENTS



7.5.2. D+/D- External Short Error Rejection

LIMITS AND RESULTS

Initial Condition: Vbus is 5 volts

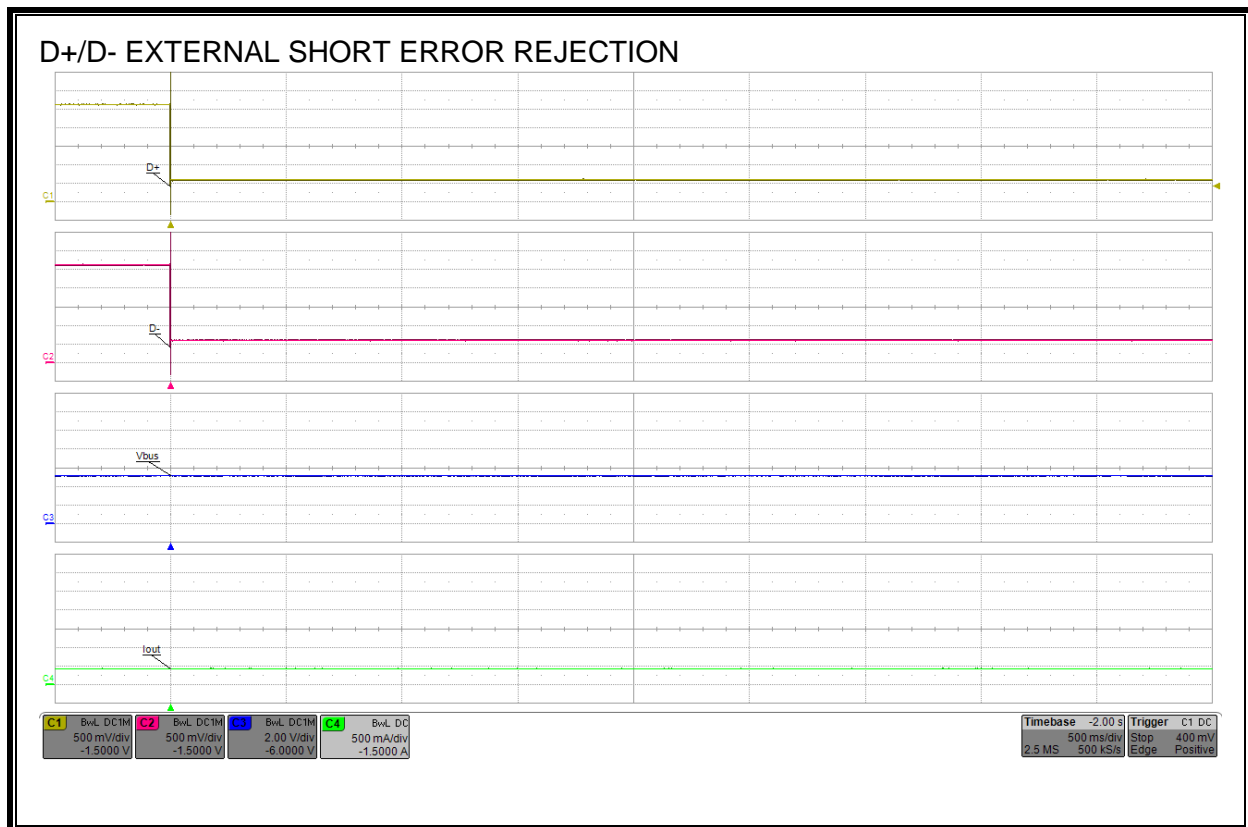
Applied Waveform: D+ and D- externally shorted together and held at 0 volts
Then 0.6 volts is applied to D+/D-

Requirement: Vbus remains at 5 volts

Observation Period: Monitor at least 2 seconds after 0.6 volts is applied

Parameter	Measured Value (V)	Minimum Limit (V)	Maximum Limit (V)	Pass/Fail
Vbus	5.165	4.75	5.50	PASS

WAVEFORM AND MEASUREMENTS



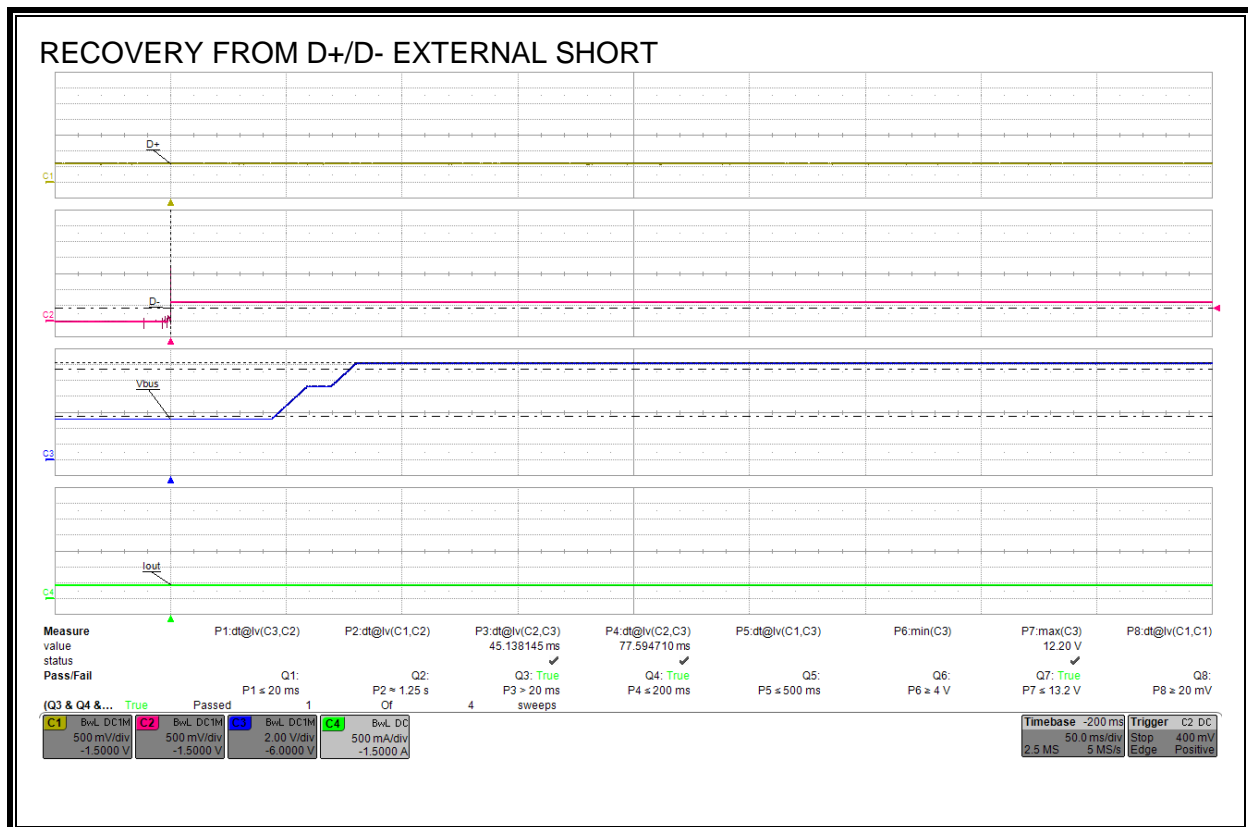
7.5.3. Recovery from D+/D- External Short

LIMITS AND RESULTS

Initial Condition: D+ and D- externally shorted together and held at 0.6 volts
Setup: Short is removed and D- allowed to float
Response: HVCDP asserts Rdm_dwn
Applied Waveform: 0.6 V is applied to D-
Requirement: Vbus makes a normal transition from 5 volts to 12 volts

Parameter	Start of Timing	End of Timing	Meas Value (ms)	Min Limit (ms)	Max Limit (ms)	Pass/Fail
Tglitch_mode_change	D- >= 0.4 V (Max Vdat_ref)	Vbus >= 5.5 V (Max Vbus_5v)	45.14	20	60	PASS
Tv_new_request	D- >= 0.4 V (Max Vdat_ref)	Vbus >= 11.4 V (Min Vbus_hv)	77.59		200	PASS

WAVEFORM AND MEASUREMENTS



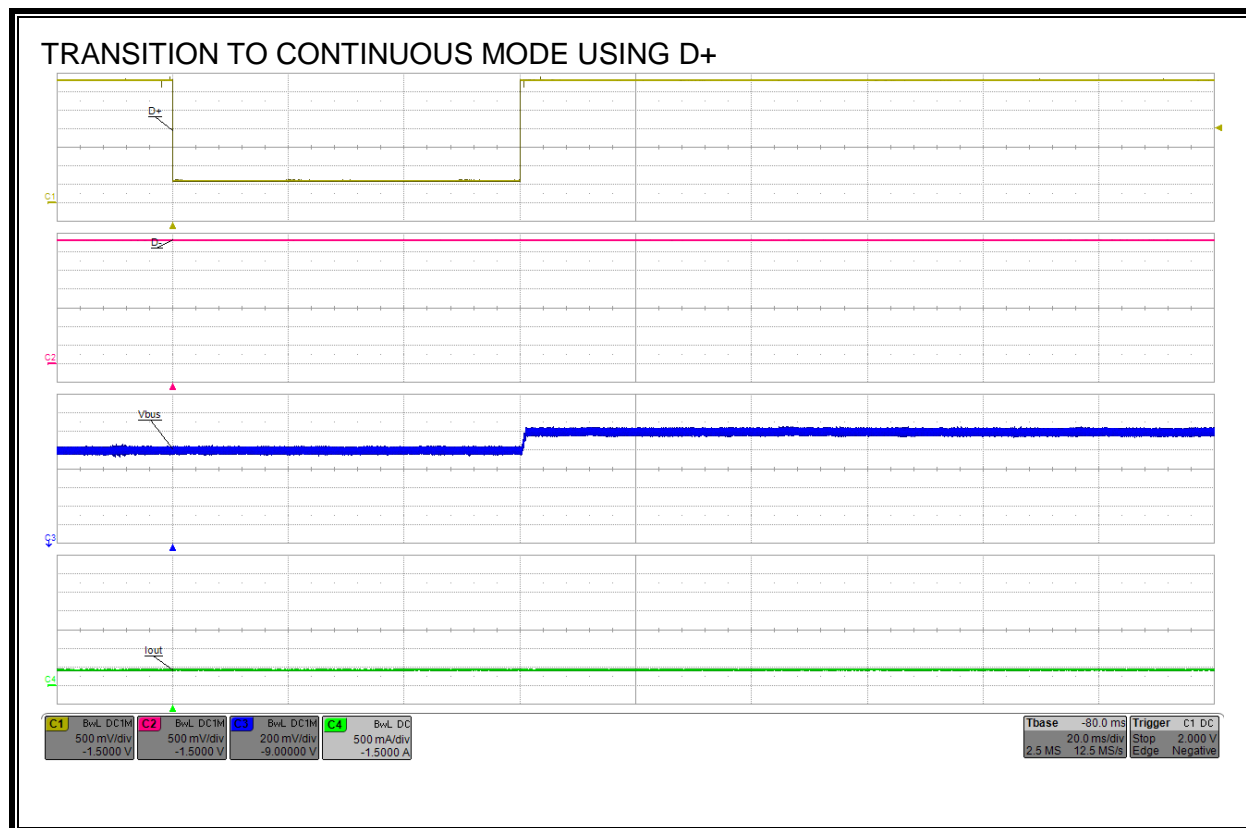
7.6. Continuous Mode Portable Device Request Recognition

7.6.1. Upper Bound of Tglitch_mode_change

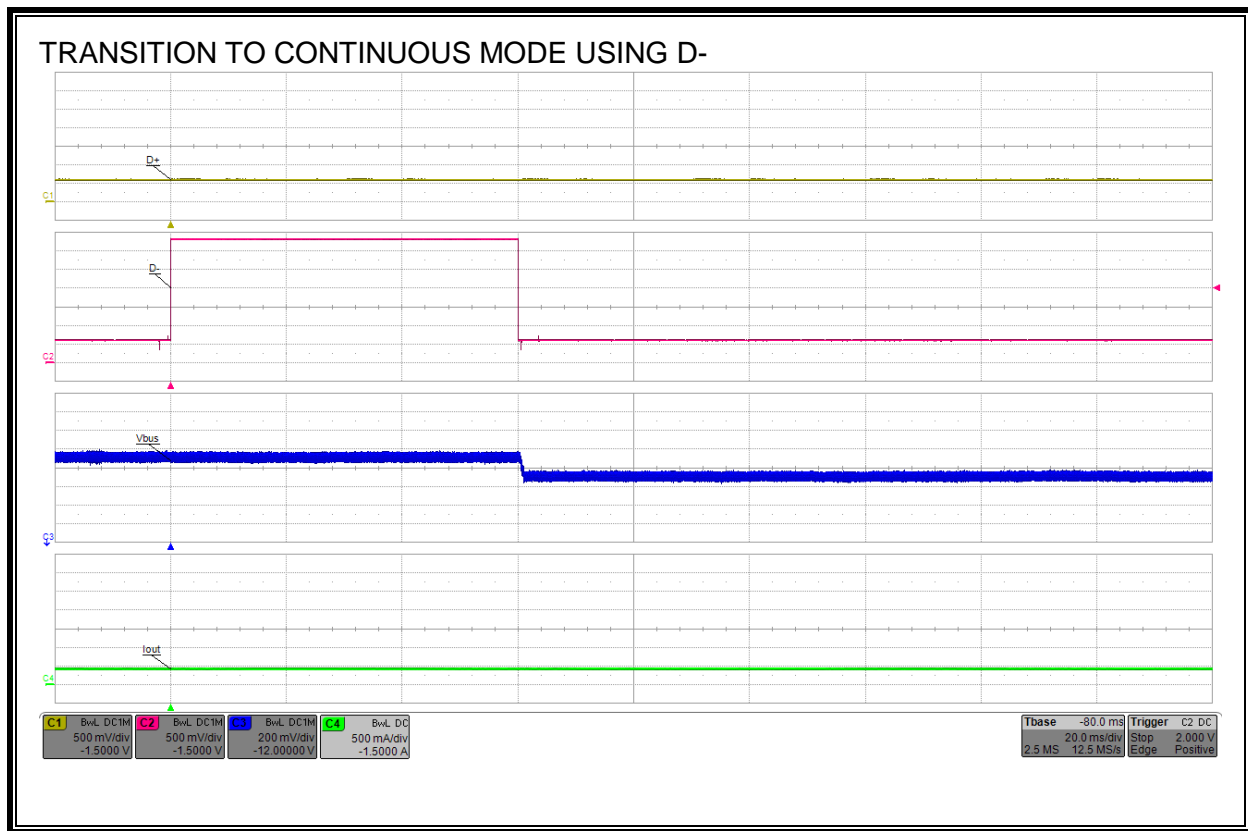
LIMITS AND RESULTS

Charger Transition	Observation of Vbus	Pass/Fail
To Continuous Mode using D+ Pulse	Increments	PASS
To Continuous Mode using D- Pulse	Decrements	PASS

WAVEFORM FOR TRANSITION USING D+



WAVEFORM FOR TRANSITION USING D-



7.6.2. Tv_cont_change & Vbus_cont_step at Upper Bound of D-Tglitch_cont_change

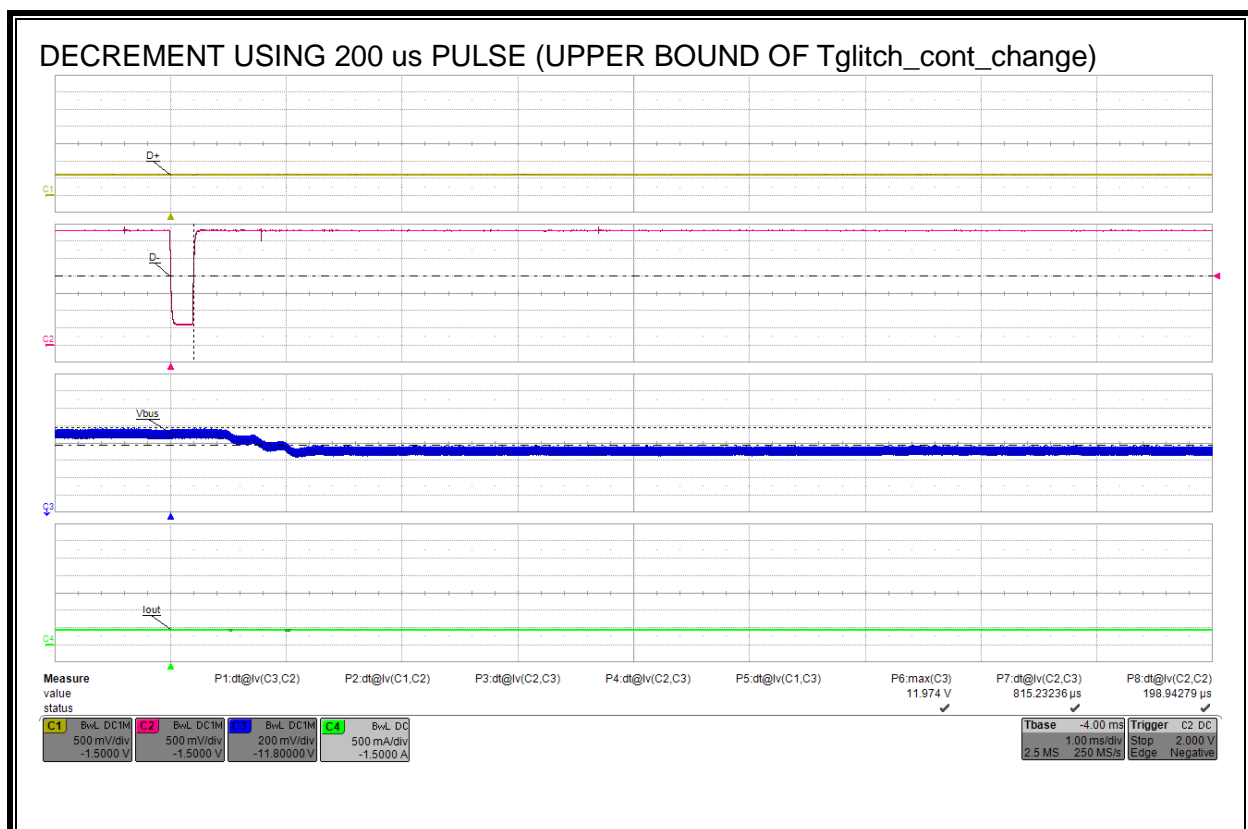
Tv_cont_change LIMITS AND RESULTS

Vbus Transition	Time from leading edge of request to completion of Vbus transition (ms)	Maximum Limit (ms)	Pass/Fail
11.8 V to 11.6 V	0.82	30.0	PASS

Vbus_cont_step LIMITS AND RESULTS

Vbus Transition	Starting Voltage (V)	Ending Voltage (V)	Delta Voltage (V)	Minumum Delta (V)	Maximum Delta (V)	Pass/Fail
11.8 V to 11.6 V	11.925	11.726	0.199	0.150	0.250	PASS

DECREMENT WAVEFORM

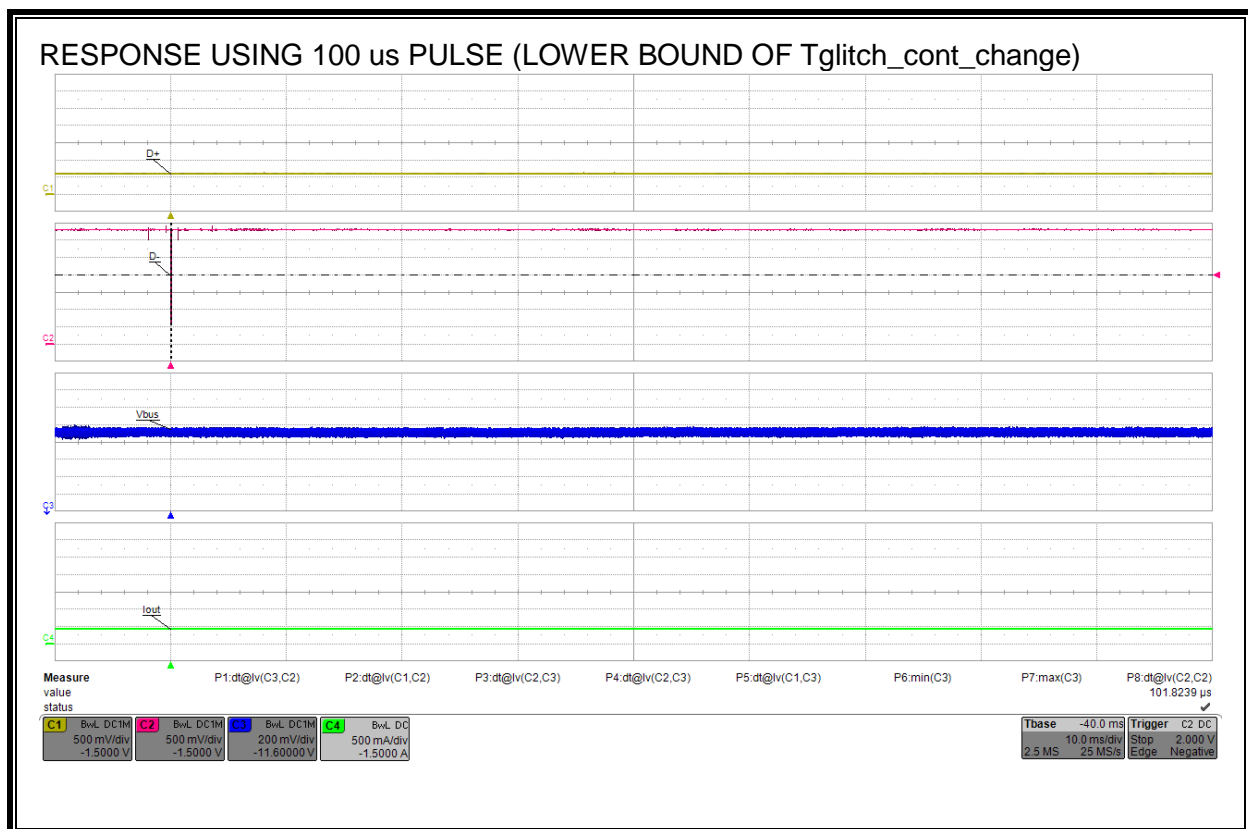


7.6.3. Lower Bound of D- Tglitch_cont_change

LIMITS AND RESULTS

D+ / D- Command	Observation of Vbus	Pass/Fail
Attempt to Decrement using D- Pulse Width < Minimum Tglitch_cont_change	Vbus does not Change	PASS

WAVEFORMS

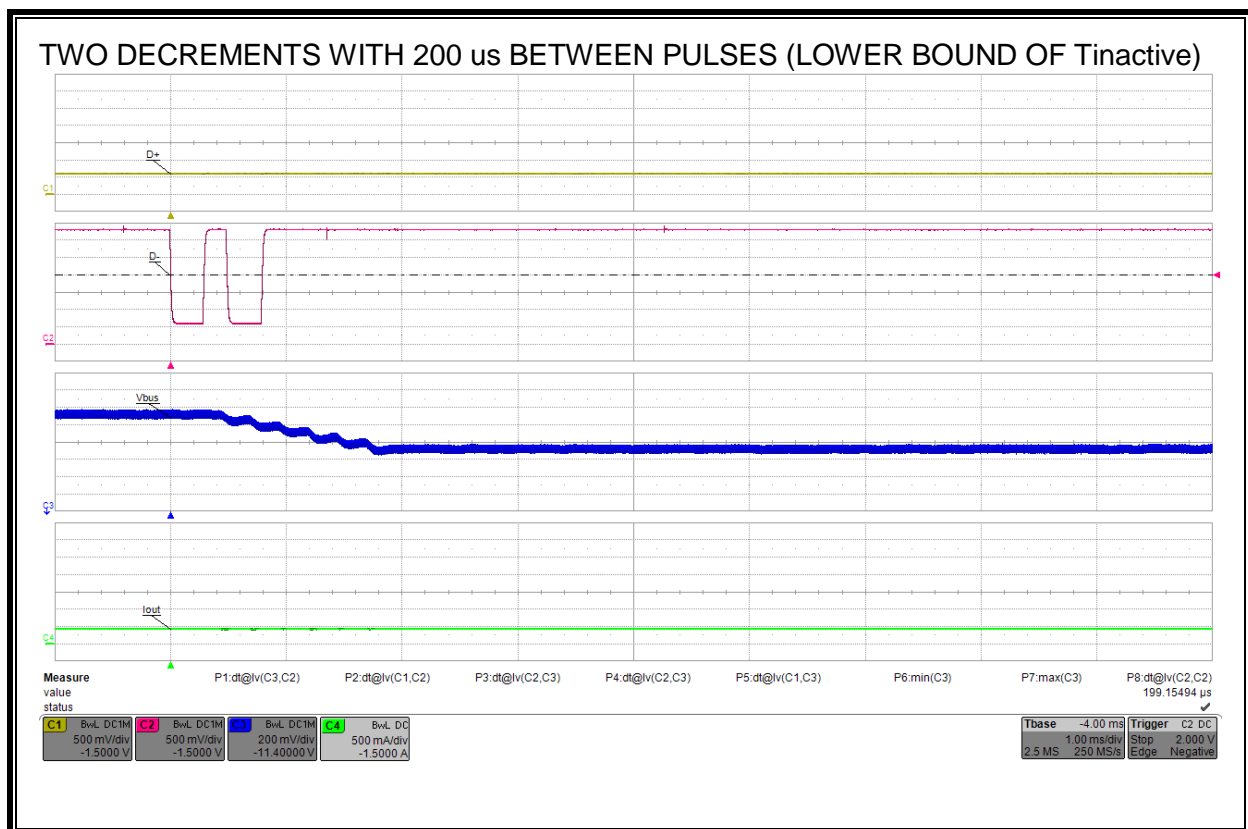


7.6.4. Lower Bound of D- Tinactive

LIMITS AND RESULTS

D+ / D- Command	Observation of Vbus	Pass/Fail
Two Decrement Pulses with minimum Tinactive timing	Vbus Decrements Twice	PASS

DECREMENT WAVEFORM



7.6.5. Tv_cont_change & Vbus_cont_step at Upper Bound of D+ Tglitch_cont_change

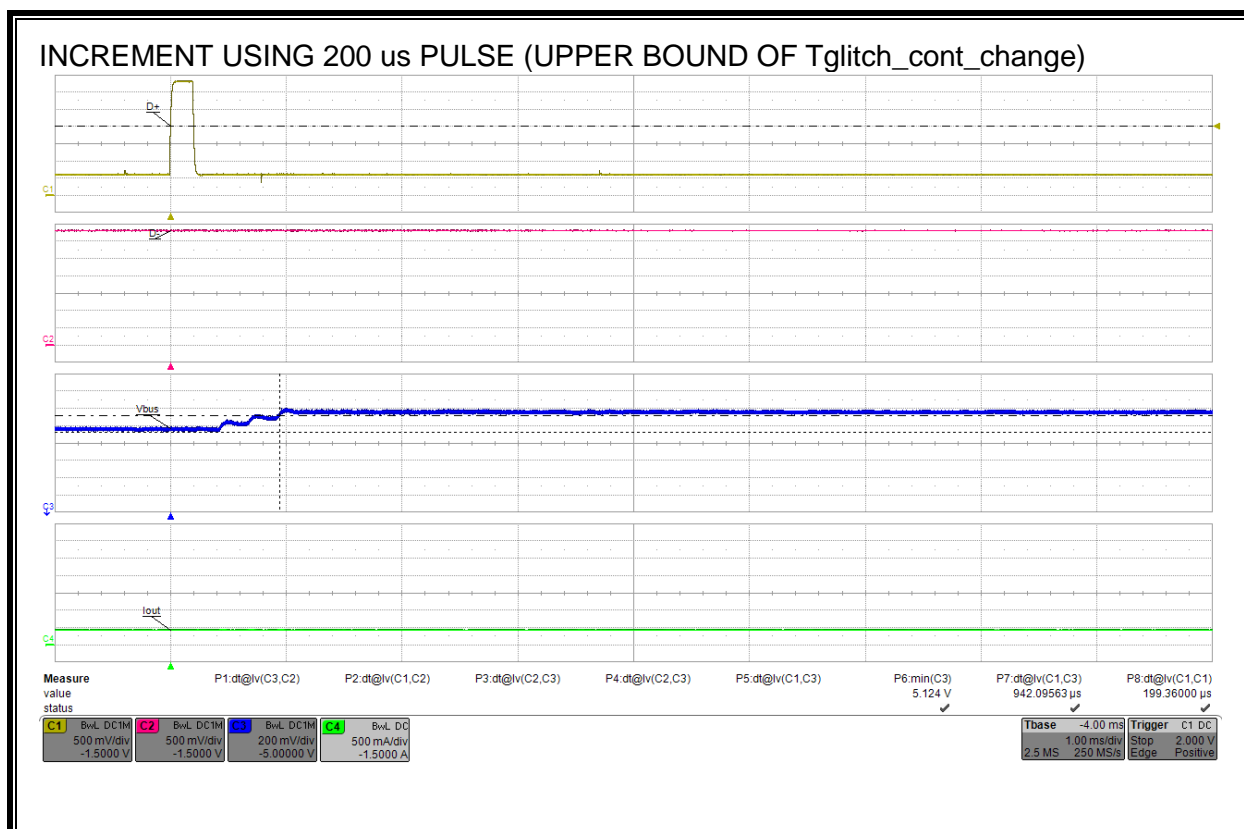
Tv_cont_change LIMITS AND RESULTS

Vbus Transition	Time from leading edge of request to completion of Vbus transition (ms)	Maximum Limit (ms)	Pass/Fail
5.0 V to 5.2 V	0.94	30.0	PASS

Vbus_cont_step LIMITS AND RESULTS

Vbus Transition	Starting Voltage (V)	Ending Voltage (V)	Delta Voltage (V)	Minumum Delta (V)	Maximum Delta (V)	Pass/Fail
5.0 V to 5.2 V	5.164	5.362	0.198	0.150	0.250	PASS

INCREMENT WAVEFORM

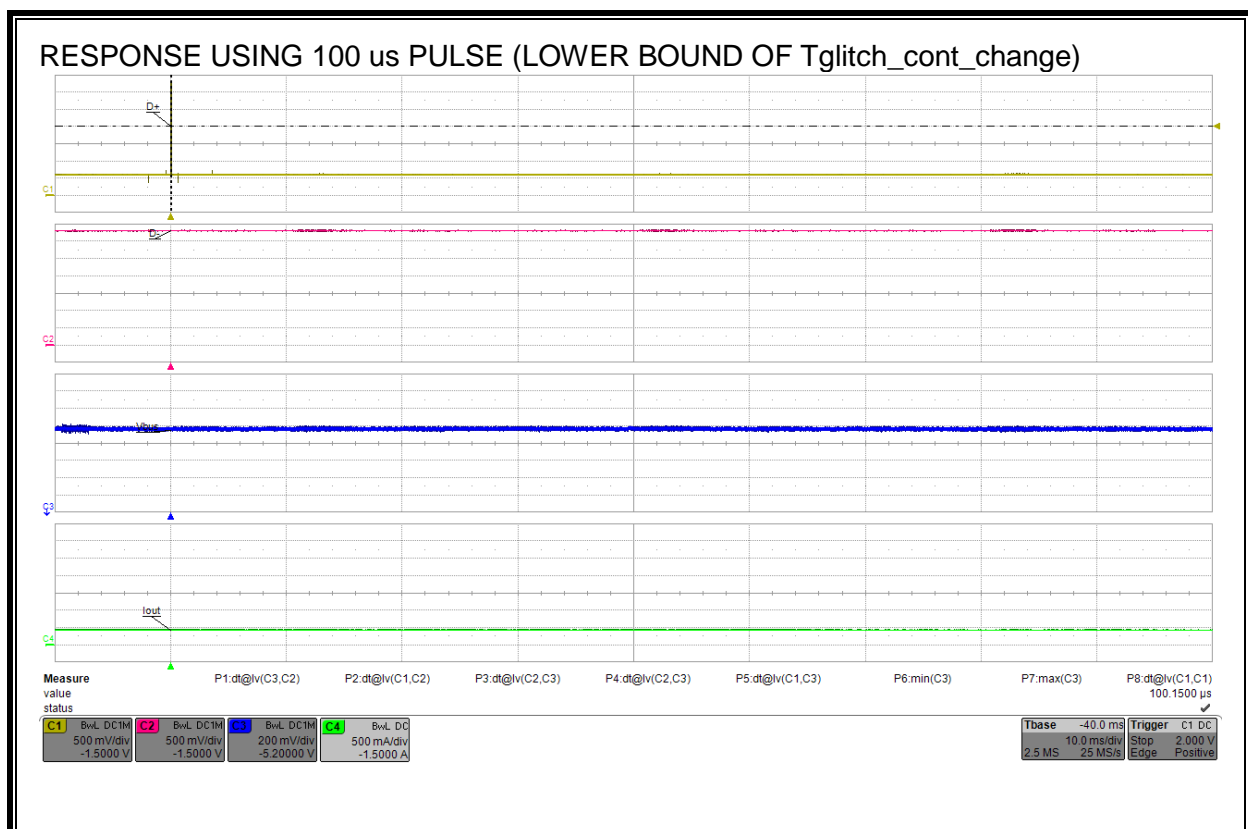


7.6.6. Lower Bound of D+ Tglitch_cont_change

LIMITS AND RESULTS

D+ / D- Command	Observation of Vbus	Pass/Fail
Attempt to Increment using D+ Pulse Width < Minimum Tglitch_cont_change	Vbus does not Change	PASS

WAVEFORMS

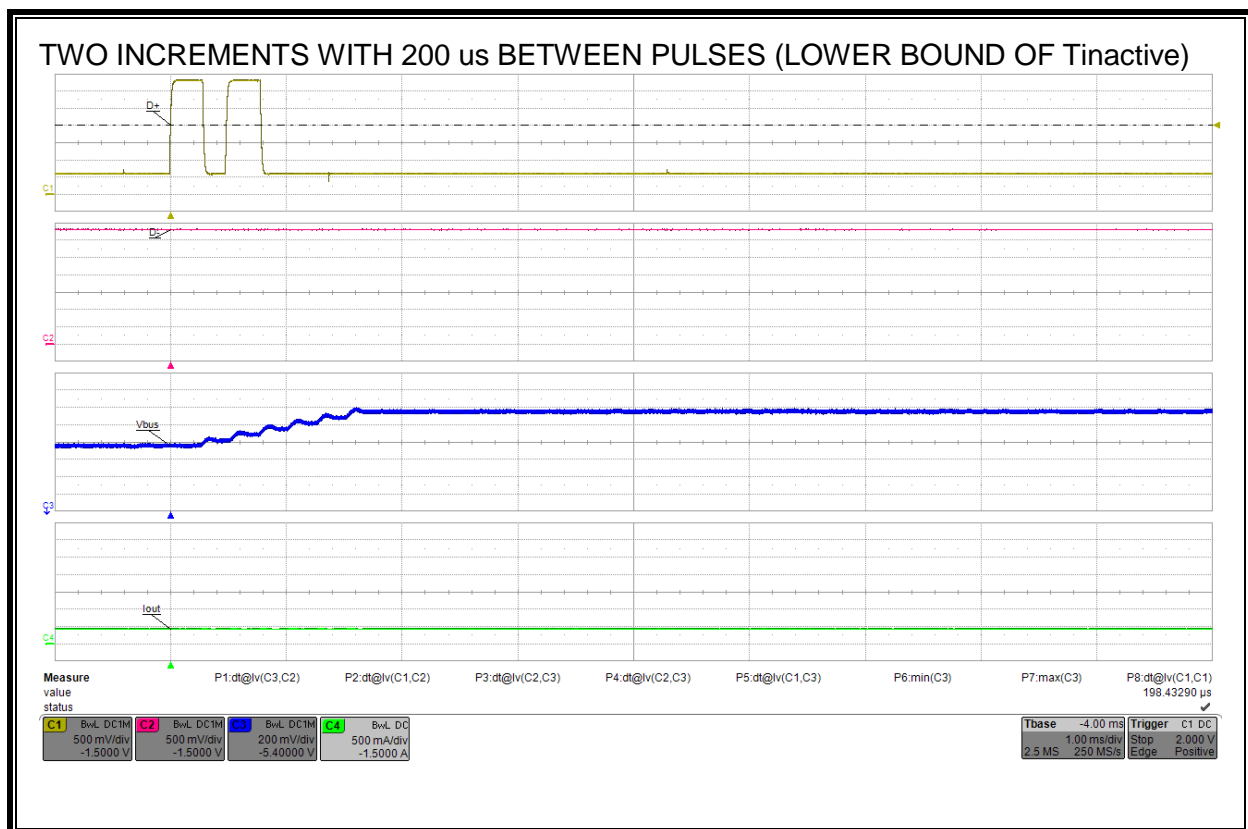


7.6.7. Lower Bound of D+ Tinactive

LIMITS AND RESULTS

D+ / D- Command	Observation of Vbus	Pass/Fail
Two Increment Pulses with minimum Tinactive timing	Vbus Increments Twice	PASS

INCREMENT WAVEFORM



7.6.8. Cumulative Tolerance of Vbus_cont_step

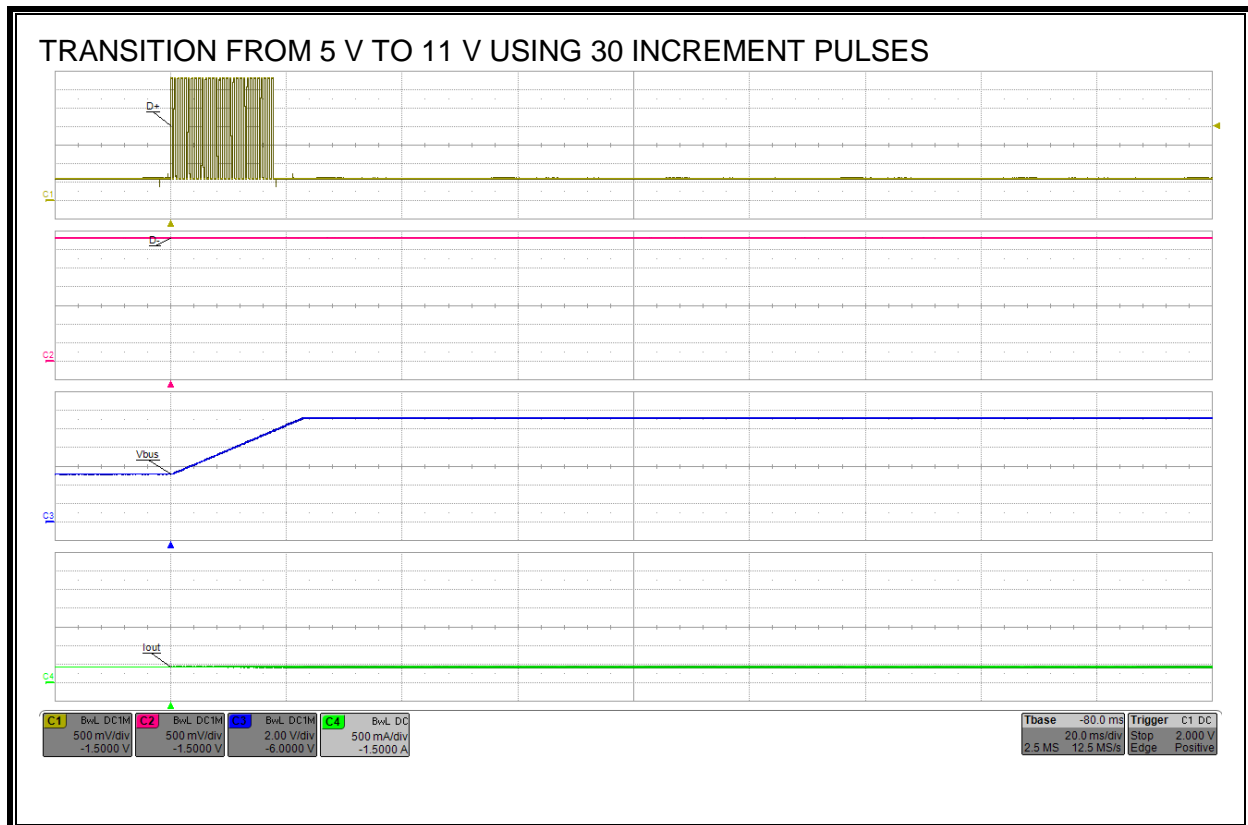
CUMULATIVE Vbus,cont,step LIMITS AND RESULTS

Requirement: Max. Tv_cont_change (30 ms) between the rising/falling edge of last pulse and the stable Vbus

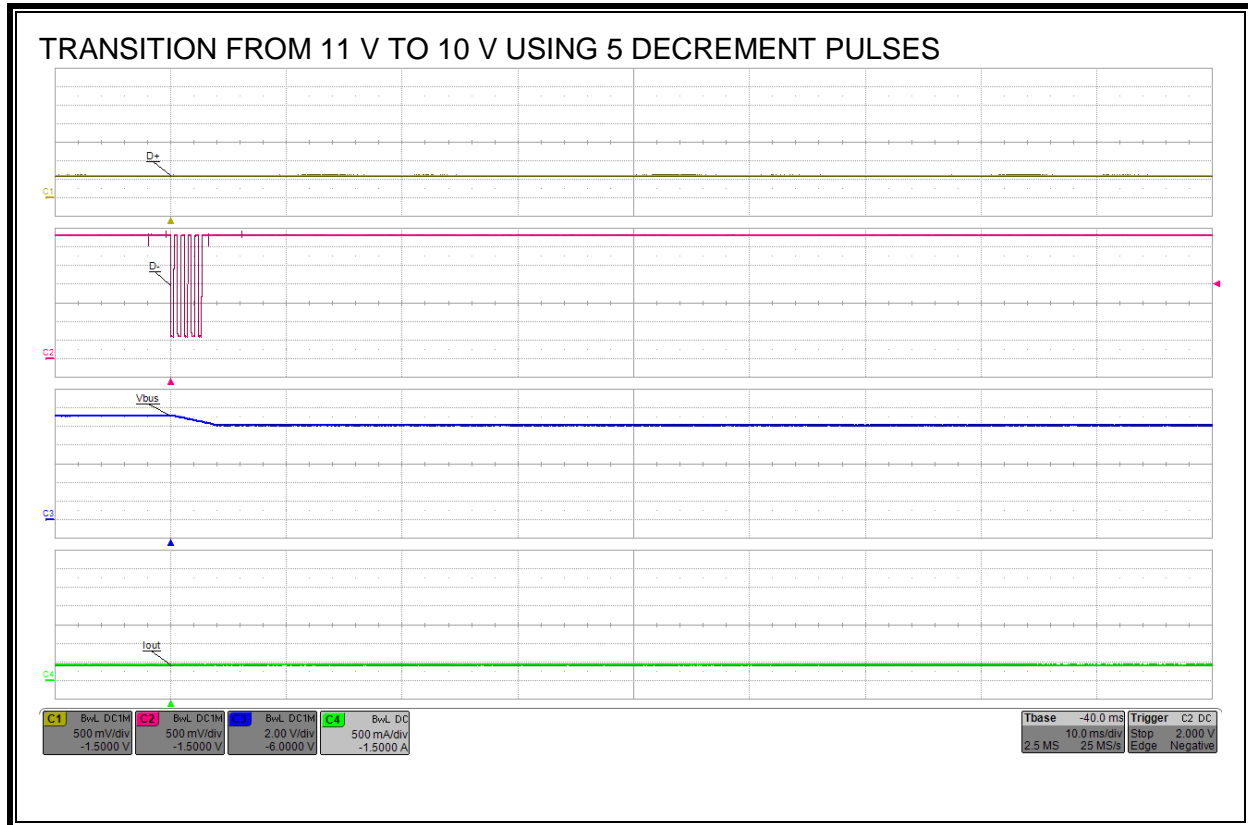
Vbus Transition	Starting Voltage (V)	Ending Voltage (V)	Delta Voltage (V)	Minumum Delta (V)	Maximum Delta (V)	Pass/Fail
5 V to 11 V	5.17	11.13	5.96	4.50	7.50	PASS
11 V to 10 V	11.13	10.13	1.00	0.75	1.25	PASS

Vbus Transition	Observation of Vbus	Pass/Fail
5 V to 11 V	Vbus does not decrement during the process	PASS
11 V to 10 V	Vbus does not increment during the process	PASS

INCREMENT WAVEFORM



DECREMENT WAVEFORM



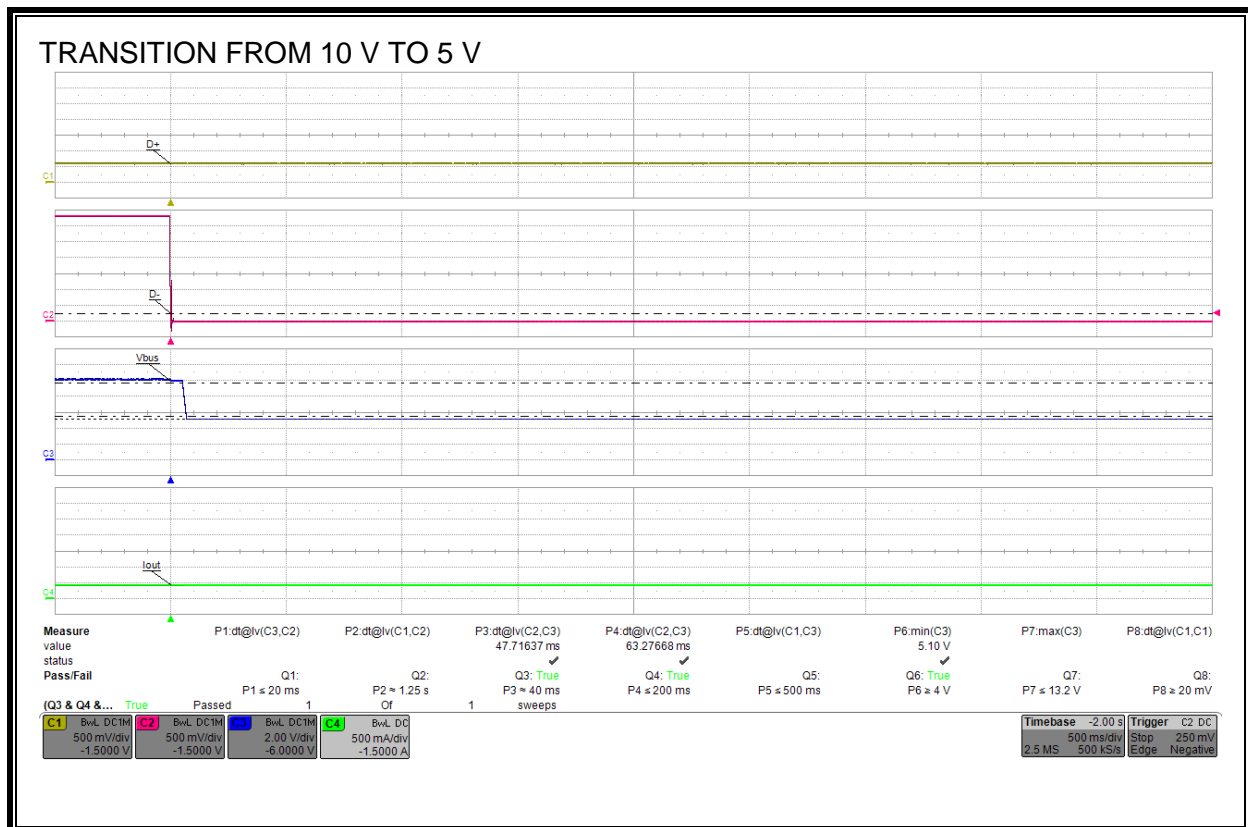
7.7. Transition from Continuous Mode to Fixed Mode

7.7.1. Transition from 10 V to 5 V

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Meas Value (ms)	Min Limit (ms)	Max Limit (ms)	Pass/Fail
Tglitch_mode_change	D- \leq 0.25 V (Min Vdat_ref)	Vbus \leq 9.6 V (Min Vbus_hv)	47.72	20	60	PASS
Tv_new_request	D- \leq 0.25 V (Min Vdat_ref)	Vbus \leq 5.5 V (Max Vbus_5v)	63.28		200	PASS

WAVEFORM AND MEASUREMENTS

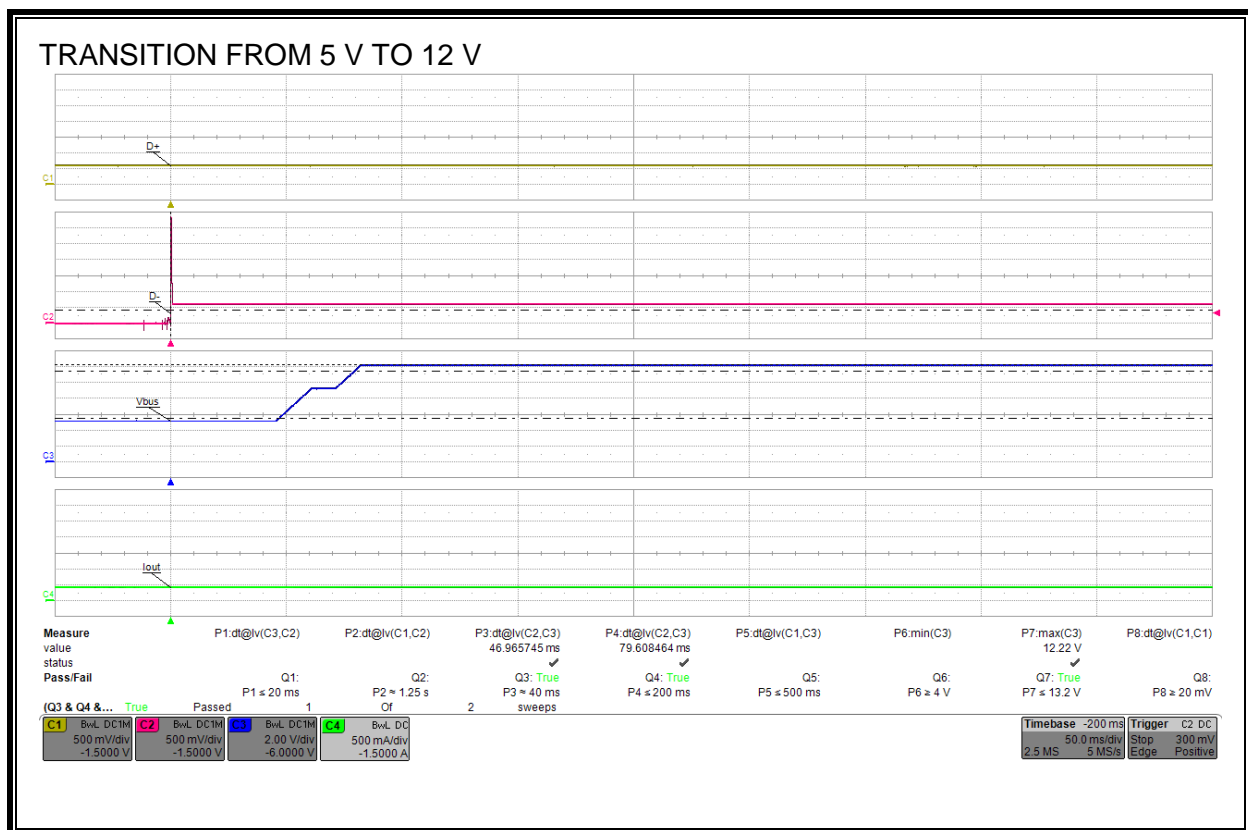


7.7.2. Transition from 5 V to 12 V

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Meas Value (ms)	Min Limit (ms)	Max Limit (ms)	Pass/Fail
Tglitch_mode_change	D- \geq 0.4 V (Max Vdat_ref)	Vbus \geq 5.5 V (Max Vbus_5v)	46.97	20	60	PASS
Tv_new_request	D- \geq 0.4 V (Max Vdat_ref)	Vbus \geq 11.4 V (Min Vbus_hv)	79.61		200	PASS

WAVEFORM AND MEASUREMENTS

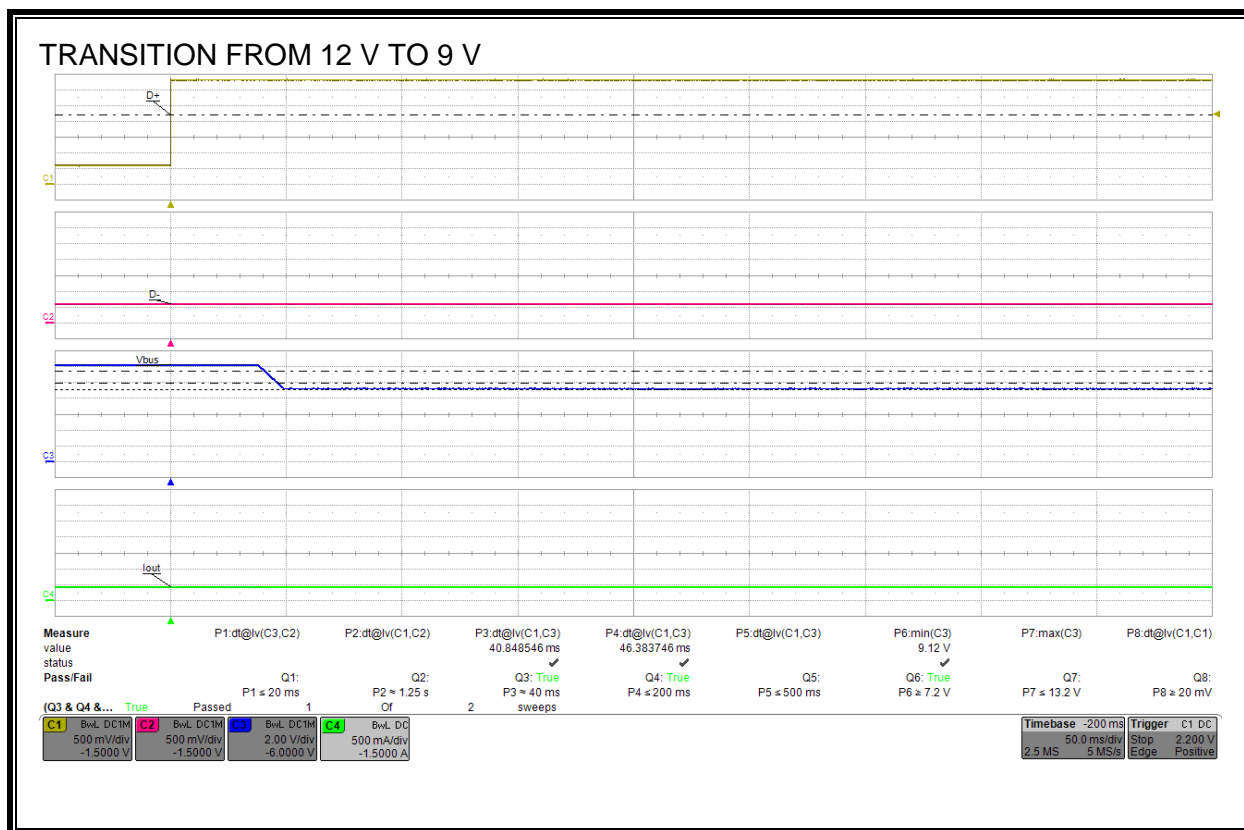


7.7.3. Transition from 12 V to 9 V

LIMITS AND RESULTS

Parameter	Start of Timing	End of Timing	Meas Value (ms)	Min Limit (ms)	Max Limit (ms)	Pass/Fail
Tglitch_mode_change	D+ >= 2.2 V (Max Vsel_ref)	Vbus <= 11.4 V (Min Vbus_hv)	40.85	20	60	PASS
Tv_new_request	D+ >= 2.2 V (Max Vsel_ref)	Vbus <= 9.9 V (Max Vbus_hv)	46.38		200	PASS

WAVEFORM AND MEASUREMENTS



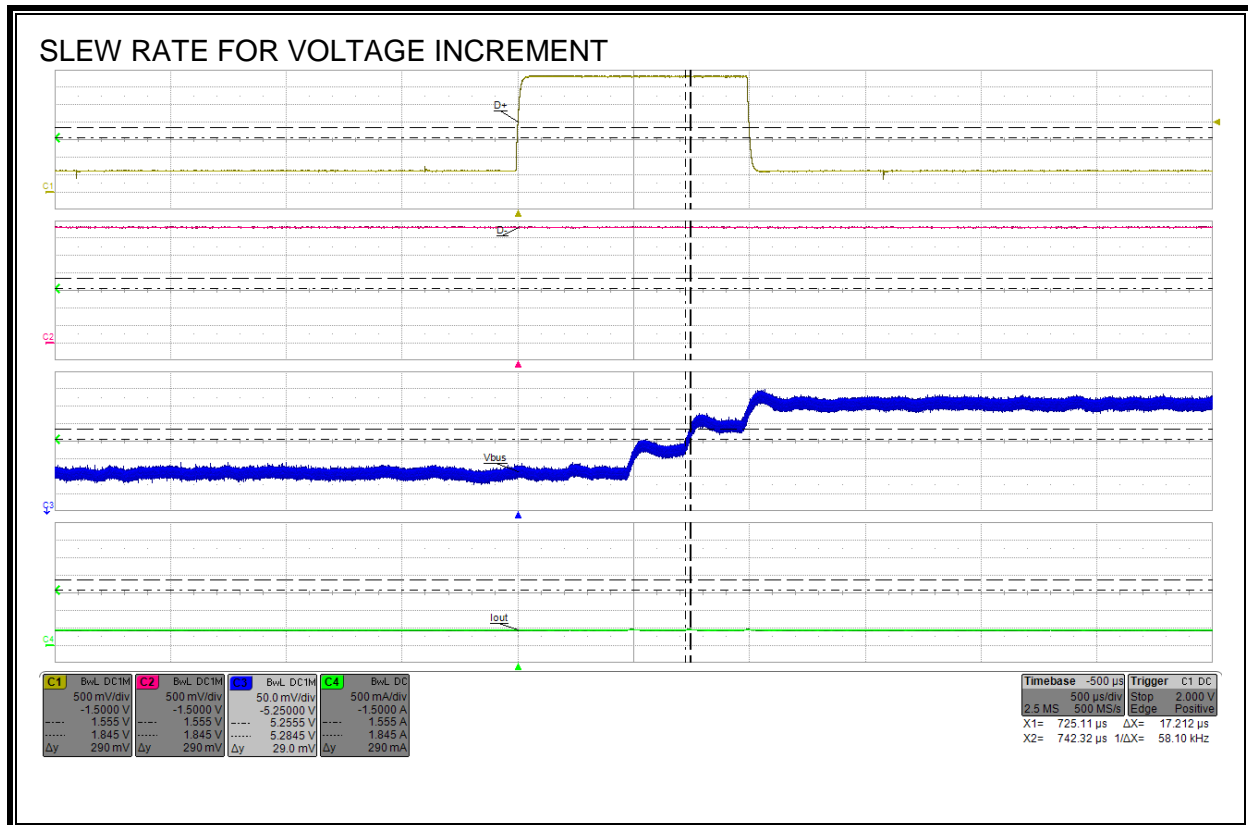
7.8. Operating Characteristics

7.8.1. Vslew_max

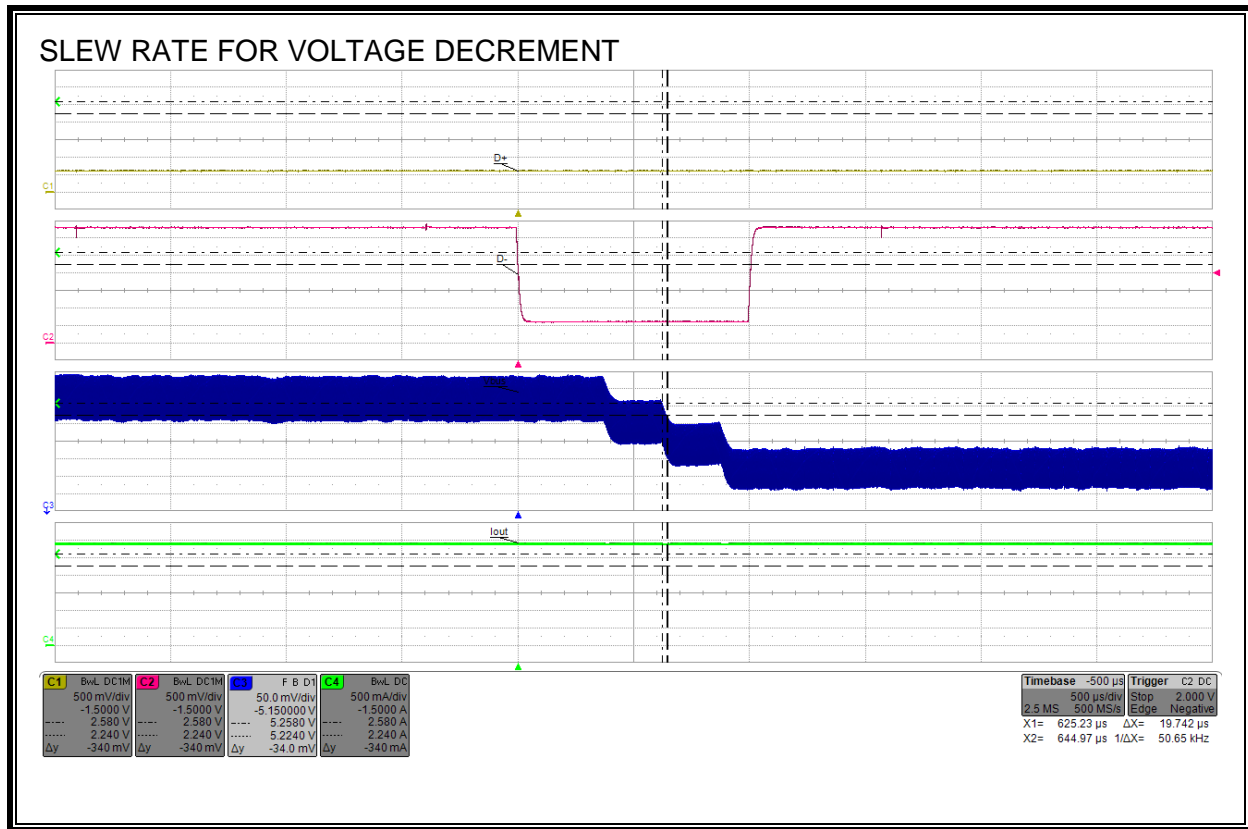
Vslew_max LIMITS AND RESULTS

Vbus Transition	Delta Voltage (mV)	Delta Time (usec)	Slew Rate (mV/usec)	Maximum Limit (mV/usec)	Pass/Fail
5.0 V to 5.2 V with 500 mA Load	29.00	17.21	1.685	30	PASS
5.2 V to 5.0 V with 3 A Load	34.00	19.74	1.722	30	PASS

WAVEFORM FOR INCREMENTING SLEW RATE



WAVEFORM FOR DECREMENTING SLEW RATE



7.8.2. Minimum Vbus_cont_range

Minimum Vbus_cont_range LIMITS AND RESULTS

Condition	Measured Value (V)
Current = 0.2 A	4.330
Current = Max Rated (3 A)	4.218

7.9. Power Profile

7.9.1. Load Point A & Minimum Pmax

LOAD POINT A LIMITS AND RESULTS

Measured Current (A)	Measured Load Point A Voltage Via Increment (V)	Measured Load Point A Voltage Via Decrement (V)	Minimum Voltage Limit (V)	Pass/Fail	Pmax (Watts)
3.00	6.283	6.283	6.00	PASS	18.85

Delta Between Via Increment & Via Decrement (V)	Delta Voltage Limit (V)	Pass/Fail
0.000	0.100	PASS

7.9.2. Load Point B

LOAD POINT B RESULTS

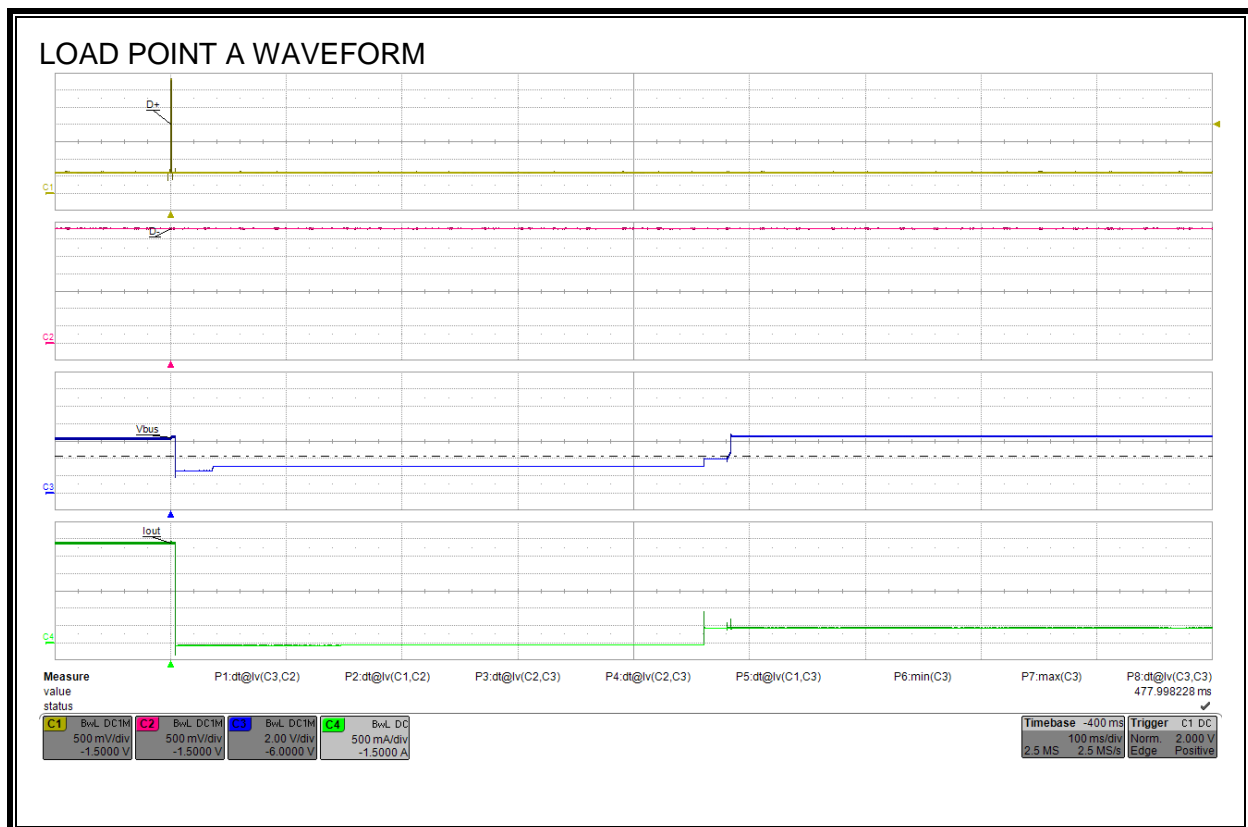
Measured Current (A)	Measured Load Point B Voltage (V)	Pmax (Watts)
2.50	6.536	16.34

7.9.3. Transition from Load Point A to Load Point B

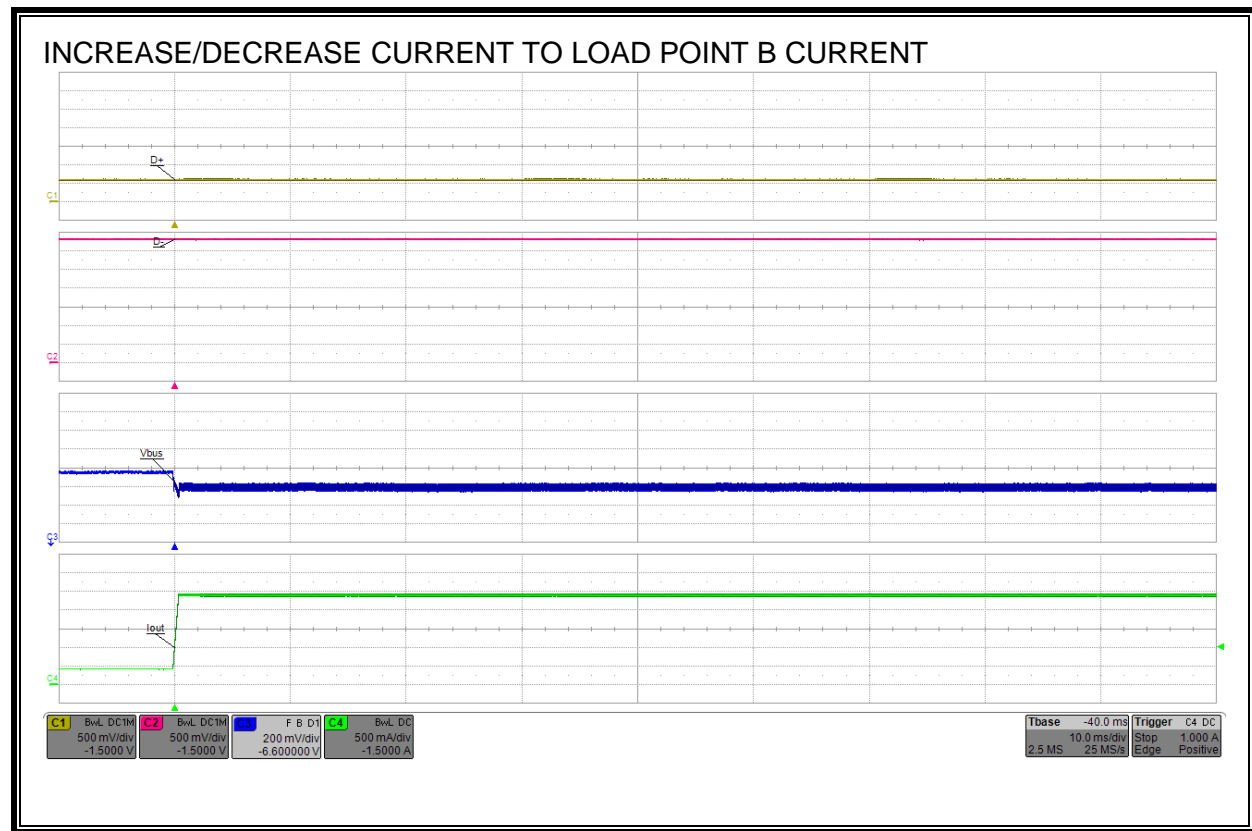
Minimum Tglitch_uvlo LIMITS AND RESULTS

Parameter	Measured Value (ms)	Minimum Limit (ms)	Pass/Fail
Tglitch_uvlo	478.00	20	PASS

VBUS REACHES LOAD POINT A

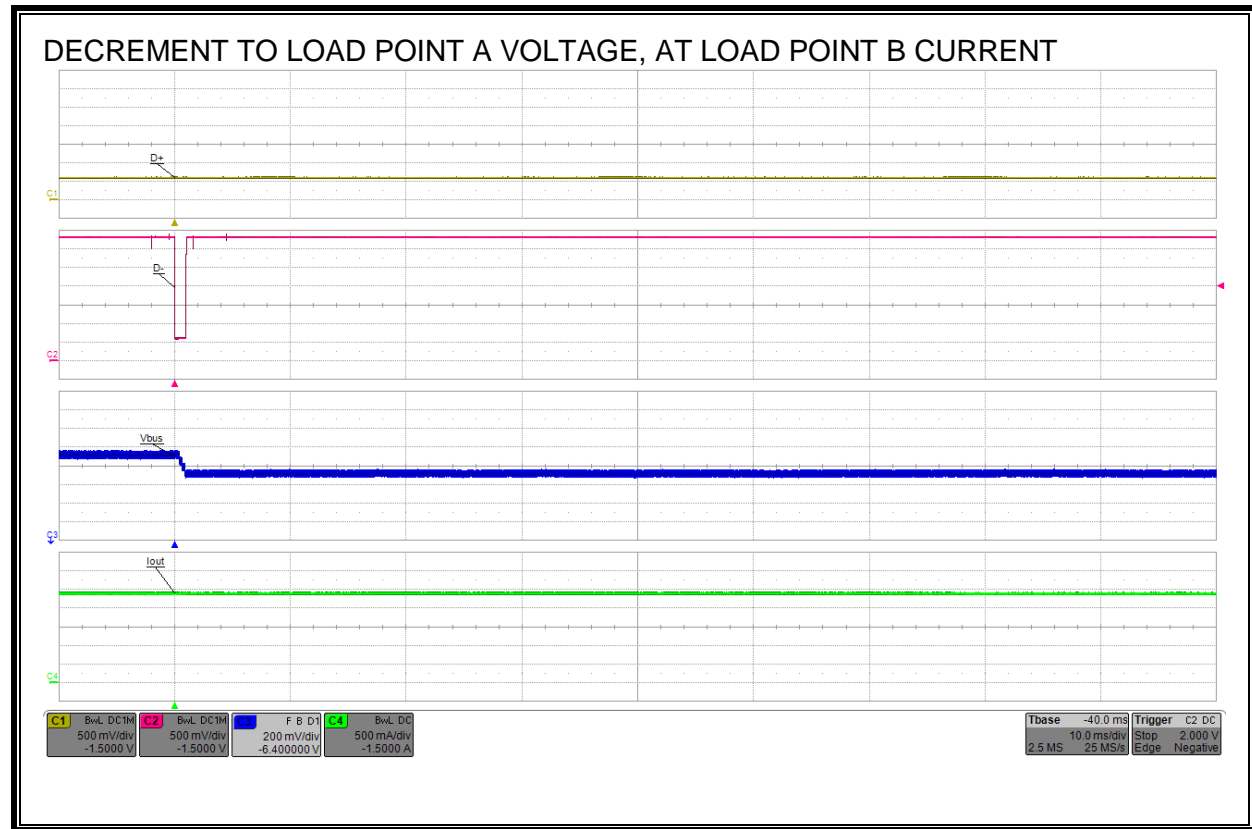


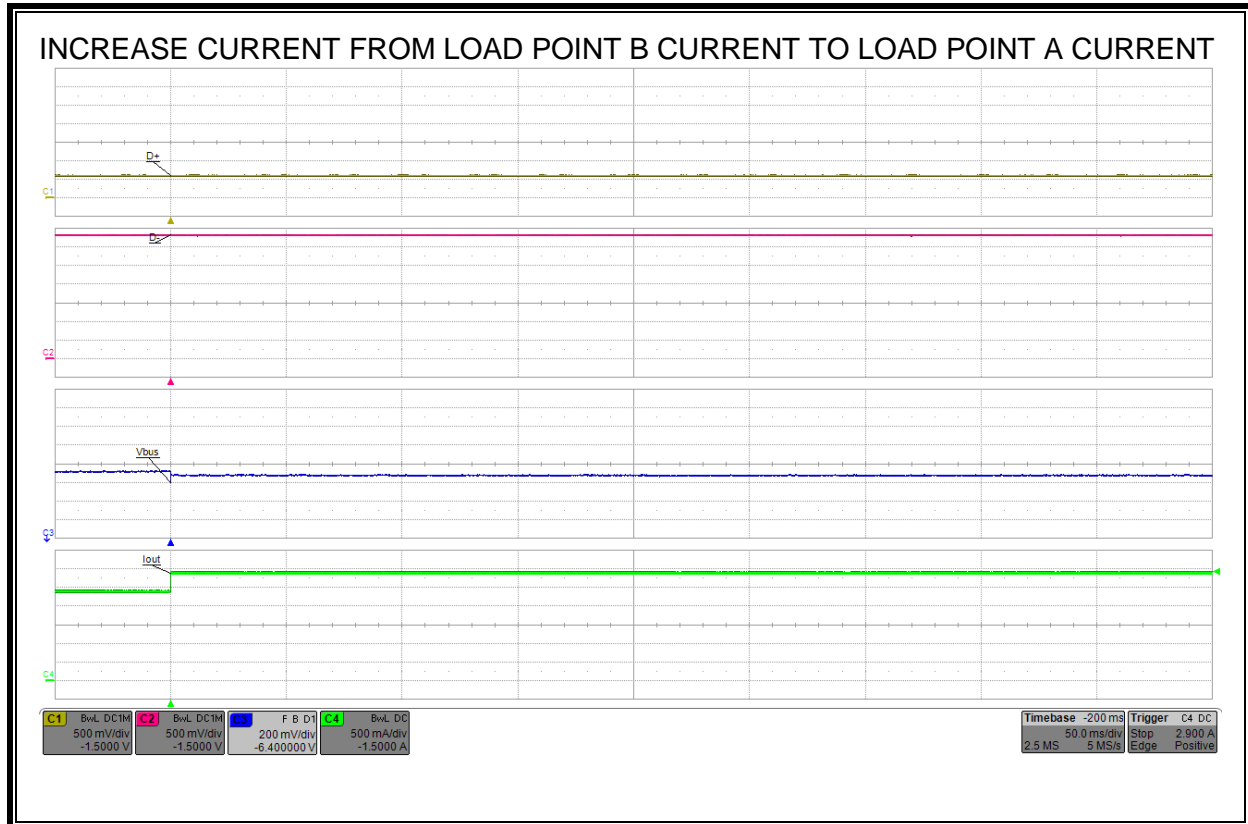
RECOVERY TO LOAD POINT B



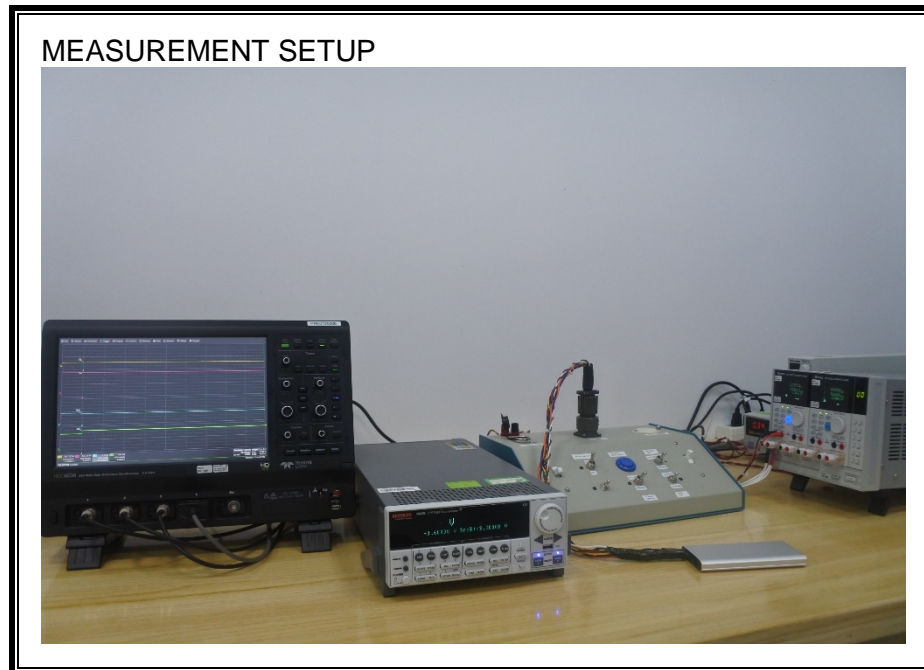
7.9.4. Transition from Load Point B to Load Point A

TRANSITION TO LOAD POINT A





8. SETUP PHOTO



END OF REPORT